V-20

HOME COMPUTER

SERVICE MANUAL

Canon

SEPT. 1984

EY8-0012-751

INDEX

I. INTRODUCTION

The V-20 home computer is an 8-bit personal computer manufactured in accordance with the MSX specifications developed by Microsoft of the United States and ASCII of Japan.
"MSX" refers to a standard aimed at providing program software compatible with all MSX machines by standardizing the different hardware and software specifications of various MSX manufacturers. By conforming to MSX standards, programs from the various companies marketing MSX equipment can be run on any MSX machine.
The V-20 comes in two versions — one is the UK version and the other is the French version. Any differences between them are specifically mentioned.

Item	French version		UK version
Top panel assy	EY7-0971-000	⋇	EY7-1091-000
Bottom panel assy	EY7-0972-000	⋇	EY7-1092-000
AC cord	EY7-1087-000	⋇	EY7-1088-000
AC switch	EY7-0920-000	⇨	EY7-0920-000
Power transformer	EY7-0921-000	⇨	EY7-0921-000
Power supply PCB	—	⇨	—
LED PCB	—	⇨	—
Keyboard assy	—	⋇	—
Key switch	EY7-0986-000	⇨	EY7-0986-000
Key switch (space)	EY7-0985-000	⇨	EY7-0985-000
Key switch (cursor)	EY7-0984-000	⇨	EY7-0984-000
Main PCB	—	⋇	
ROM	EY7-0942-000	⋇	EY7-1095-000
RF modulator	None	⋇	EY7-0970-000

Note:
The ⇨ mark indicates parts that are interchangeable and the ⋇ mark indicates those that are not.

I-1. SPECIFICATIONS

CPU	8-bit Z-80A or equivalent
Clock	3.579545 MHz
VDP VIDEO CHIP	TMS-9929A
Text	32 characters x 24 lines
Graphics	256 x 192 pixels
Colours	16
PROGRAM SOUND GENERATOR	YM2149
Scale	8 octaves, 3-tone chord (+ special effects)
ROM	Type 23256
Capacity	32 K (MSX BASIC)
RAM	
System RAM	64 K (Type 4864)
Video RAM	16 K (Type 4116)
KEYBOARD	
Keys	73 (UK version) 72 (French version)
CARTRIDGE SLOTS	2
CASSETTE INTERFACE	Remote control function
Modulation	FSK system
Transmission speed	1,200/2,400 baud
PRINTER INTERFACE	8-bit parallel interface BUSY, STROBE, handshake
TV INTERFACE	
VIDEO OUT	Composite video signal (UK version) RGB signals (French version)
RF OUT	UHF 36 channel (UK version)
POWER REQUIREMENTS	AC 230 V ±10%
DIMENSIONS	402 (W) x 218 (D) x 62 (H) mm
WEIGHT	2.5 kg

I-2. INTERFACES

The unit's interfaces are shown in Fig. I-1.

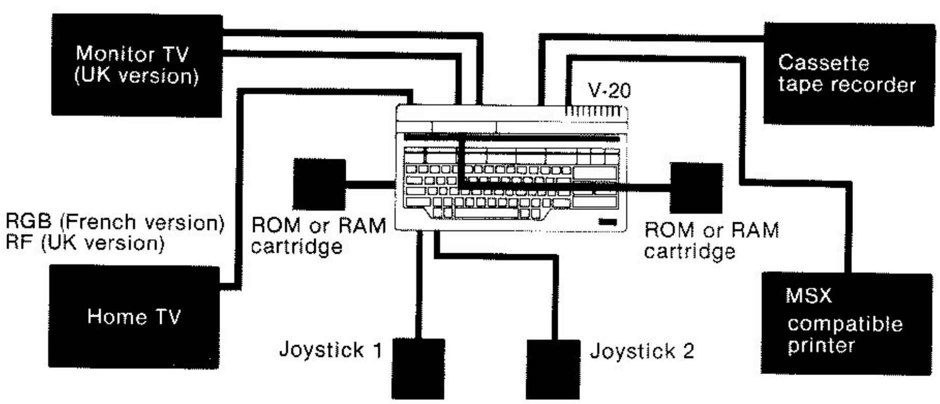


Fig. I-1

I-3 PARTS

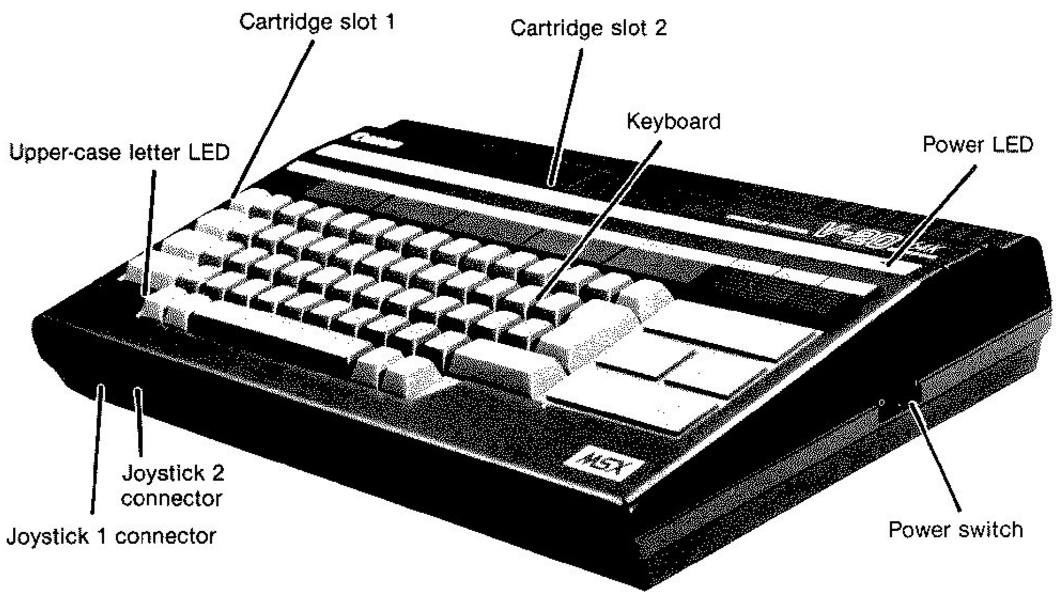


Photo I-1

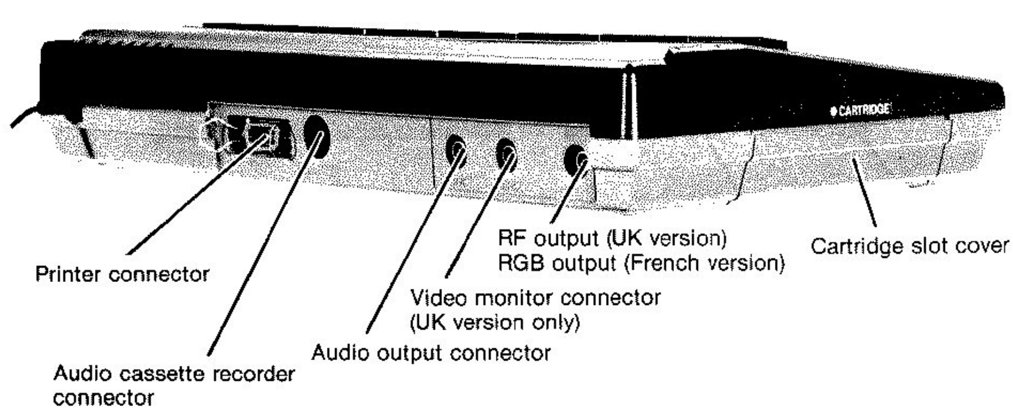
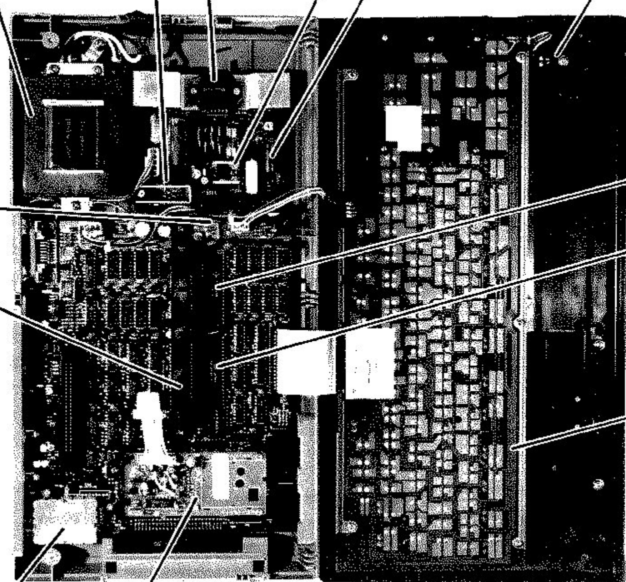


Photo I-2



−12 V regulator IC
+5 V regulator IC
+12 V regulator IC
Secondary fuse
Power transformer
LED PCB
VDP
VDP crystal
PPI
CPU
Keyboard
RF modulator
(Not used in French version)
PAL encoder PCB
(RGB encoder PCB in French version)
Note: Under this PCB, ROM and PSG are mounted.

Photo I-3

II. MAINTENANCE

This chapter details the disassembly, re-assembly and adjustment procedures required for normal maintenance.
The adjustments represent the minimum conditions for proper operation of the unit and so when trouble occurs, it is recommended that an inspection be carried out first.

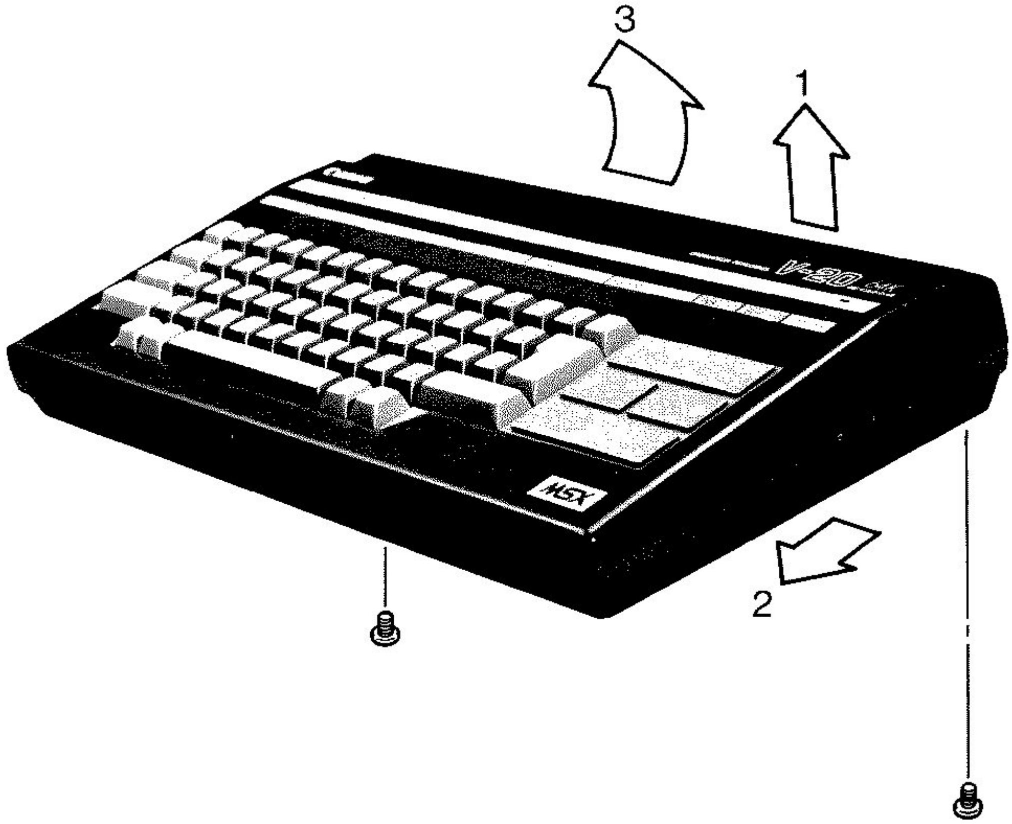
II-1. CAUTION

- Make absolutely sure that the power switch has been set to the OFF position and then that the AC cord has been disconnected from the power outlet before proceeding with disassembly.
- The following points should be borne in mind when handling MOS ICs since their structure makes them prone to damage by static in clothes or the body:
  - * Wrap the MOS ICs and main PCB in aluminum foil when storing or transporting these parts.
  - * Use a well-grounded soldering iron. If an ungrounded soldering iron is used, check that there is no leakage from the iron tip using a tester.
  - * If possible, use a work bench which is charge-proof.
- For safety reasons, use parts with identical characteristics for the parts on the power PCB and for C5, C18, C35, R15 and D4 on the main PCB.

II-2. DISASSEMBLY PROCEDURES

Top and bottom panels

Remove the two screws at the far side of the bottom panel, lift up the far side of the top panel, pull it toward you and then lay it face down. Do this carefully because of the connectors which connect the keyboard and main PCB on the near side.



Keyboard

Disconnect the power LED connector and JN1 and JN3 on the main PCB. Remove the five screws securing the keyboard and top panel and also the two keyboard holders.

Power PCB

Disconnect CN1 and connector J7 on the main PCB; then remove the screw which secures the power PCB to the bottom panel.

Encoder PCB

Disconnect all connectors between Main PCB and this PCB. Then remove the two screws securing this PCB.

Main PCB

After having disconnected all the connectors and the ground wire soldered at R31, remove the five screws securing the main PCB to the bottom panel. This can be done, while exercising caution with the printer connector holder, by lifting the near side of the PCB, sliding it toward you and freeing the main PCB from the bottom panel.

II-3. RE-ASSEMBLY CHECKPOINTS

Basically, the disassembly procedure is followed in reverse for parts re-assembly but the following points should be borne in mind.

Main PCB
Exercise care with the ground wire mounting and printer connector holder.

Power PCB
When inserting the PCB, align the cutout and bottom panel tab.

Keyboard
When inserting the flat cable from the keyboard into JN1 on the main PCB, take care not to allow the signal pattern on the cable to peel off.

Top and bottom panels
Position the power cord stopper so that the flat part of the bellows is placed perpendicularly and the part where the groove forms a semi-circle is on the top panel side. Set the power switch so that the green marker is on the near side. Position the top panel so that it fits into the tabs provided on the near side and left and right of the bottom panel.

II-4. ADJUSTMENT PROCEDURES

The unit's +5 V voltage and VDP clock can be adjusted. Before proceeding, however, check that the supply voltage is ±10% of the rating.

+5 V voltage adjustment

Measure the voltage at pin 1 (+5 V, brown) and pin 4 (GND, black) of the connector inserted into the main PCB J7 from the power PCB and adjust VR1 on the power PCB to set this voltage to +5±0.25 V.

VDP clock adjustment

Using a 10:1 probe, connect a frequency counter to pin 37 of U30 (VDP) on the main PCB. Adjust TC1 to set the frequency to specified value.

UK version: 445.12~445.52 kHz

French version: 447.3~447.7 kHz

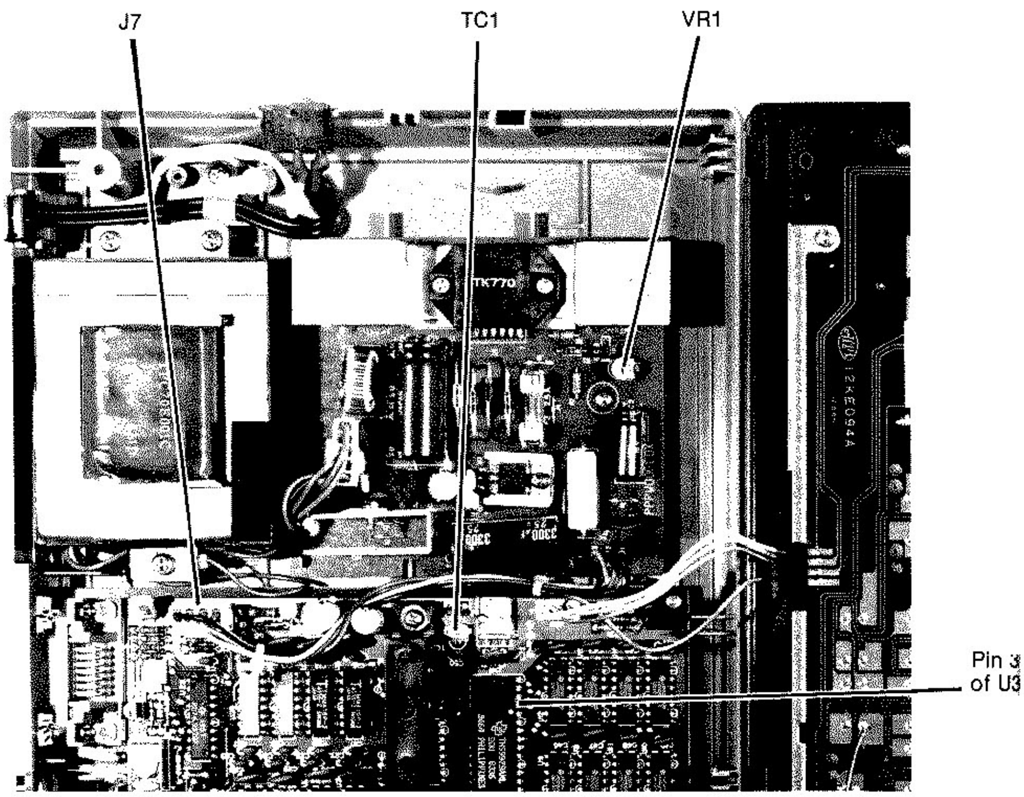
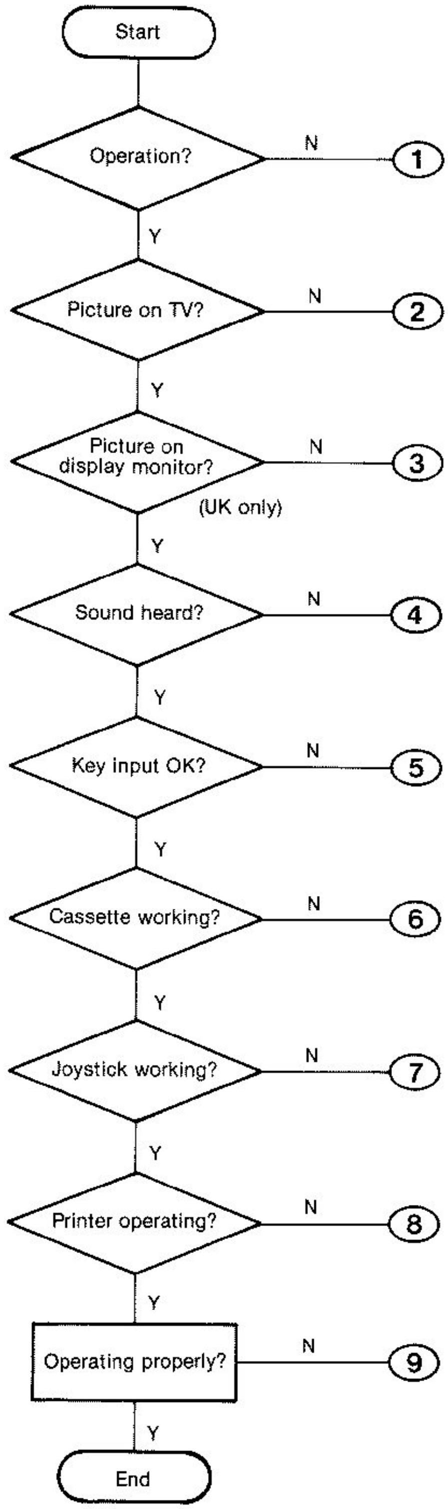


Photo II-4

II-5. TROUBLESHOOTING



①

Power check

1. Is power cord connected to power outlet?
2. Is power switch at ON position?
3. Is power LED on?

Power circuit check

1. Has fuse blown? (F2 = 2.5 A)
2. Is connector CN1 on power PCB connected?
3. Is connector J7 on main PCB connected?
4. Is +5 V voltage being supplied?
   <Check Procedure>
   (1) Set the power switch to ON.
   (2) Locate the four DC output wires leading from the power PCB. (J7)
       Brown: +5 V
       Red: +12 V
       Orange: −12V
       Black: GND
   (3) Connect a tester to J7 and check that the voltage is +5 V ±5%.
   (4) Check the parts used for the +5 V circuit:
       C1~C3, D1~D5, R1~R6, TR1, U1, VR1, L1, C10, C11
       Refer to II-4 if the voltage is not +5 V ±5%.
5. Is +12 V voltage being supplied?
   <Check Procedure>
   (1) Set the power switch to OFF.
   (2) Disconnect the J7 connector on the main PCB.
   (3) Check the parts used for the +12 V circuit:
       C4~C6, U2, D6, R8
6. Is −12 V voltage being supplied?
   <Check Procedure>
   (1) Set the power switch to OFF.
   (2) Disconnect the J7 connector on the main PCB.
   (3) Check the parts used for the −12 V circuit:
       C7~C9, U3

Main PCB check

1. Is the master oscillation frequency 14.31818 MHz?
   Measure the frequency at U49 pin 3 with an oscilloscope.
2. Is the CPU clock "ϕ" frequency 3.579545 MHz?
   Measure the frequency at U3 pin 6 with an oscilloscope.
3. Reset circuit check
   Is U3 pin 26 high?
   Check D5, C36, R19~R22, TR3, U41.
4. CPU peripheral circuitry check
   (1) Address bus area (A0~A15)
   U4, U5, U51
   (2) Data bus area (D0~D7)
   U23
   (3) Control signal area
   U40
5. Cartridge signal check
   CN1, CN2
6. Is the −5 V voltage supplied?
   <Check Procedure>
   (1) Is the −12 V voltage being supplied?
   (2) Measure the voltage at U31~U38 across pin 1 and GND using a multimeter.
   (3) Check the parts used in the −5 V circuit.
   R15, D4, C18
7. Main RAM area check
   (1) Dynamic RAM check
   U8~U15
   (2) RAM address multiplexer check
   U6, U7
   (3) $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ check
   U25, U41~U44, U46, U47
   (4) SLTSL3 area check
   U16~U18
8. PPI area check
   (1) I/O decoder circuit check
   U18, U22, U28, U41, U43
   (2) Control outputs from U3
   $\overline{M1}$, $\overline{IORQ}$, $\overline{RD}$-N, $\overline{WR}$-N

9. ROM area check
   (1) Address inputs (A0~A15)
   (2) Data outputs (D0~D7)
   (3) $\overline{\text{SLTSL0}}$
10. Wait circuit check
   (1) ϕ input
       U1
   (2) External $\overline{\text{WAIT}}$
   (3) $\overline{\text{M1}}$
       U40
11. Others
   (1) Data bus
       I/O interface IC, U18, U24, U29, U30
   (2) I/O control address
       A0, A1, A14, A15

②

TV connections check

1. Is cable connected correctly?
2. Is the channel selector set correctly?

Computer internal check

1. Encoder PCB check
   (1) UK version
       Check RF modulator
       Check PAL encoder PCB
       Check connector JN10
   (2) French version
       Check RGB encoder PCB
       Check connectors JN10 and JN12
2. VDP area check
   (1) VDP
       U30
   (2) I/O decoder circuit
       U18, U22, U28, U41, U43
   (3) Crystal
       Frequency check (Refer to II-4)
   (4) Video RAM check
       U31~U38
   (5) Control signal and data bus from CPU

③ **(UK version only)**

TV connections check

1. Is cable connected to VIDEO output?
2. Is connection made to the VIDEO input on the TV?
3. Is TV connection for composite video input?
   * Some monitor displays allow only specific TV signal input.

Computer internal check

1. Video output pin
   J6
2. Composite video circuit
3. VDP area check
   (1) VDP
       U30
   (2) I/O decoder circuit
       U18, U22, U28, U41, U43
   (3) Crystal
       Frequency check (Refer to II-4)
   (4) Video RAM check
       U31~U38
   (5) Control signal and data bus from CPU
4. PAL encoder PCB.

④

Home TV

1. Check again items listed in Section ②.
2. Adjust the volume control on the TV.

Monitor display

1. Is TV's AUDIO input connected to computer's AUDIO output?
2. Is cable connected to AUDIO output?
3. Adjust the volume control on the TV.

Audio system (amplifier)

1. Is system's AUDIO input connected?
2. Is system's input selector set properly?
   * Some amplifiers have a function selector.
3. Is the volume control set appropriately?

Computer interior

1. Check the connectors.
   J2
2. Check the mixing circuit.
   U50
   −12V check

3. PSG area check
   (1) PSG
       U24
   (2) Clock input check
   (3) Control signal check
       U2, U21, U24, U46, U43
   (4) I/O decoder circuit
       U22, U41, U43
   (5) Addresses A0, A1 and data bus from CPU

⑤

No input from any key

1. Check the connector connection.
2. Check keyboard control circuit.
   U18, U19
3. Check I/O decoder circuit.
   U18, U22, U28, U41, U43
4. Check control signal output from U3.
   $\overline{M1}$, $\overline{IORQ}$, $\overline{RD}$-N, $\overline{WR}$-N

No input from some keys

1. Check the connector connection.
   JN-1
2. Check strobe signal output.
   JN-1, U19, U18 PC port pins 14~17, U52
3. Check return signal.
   JN-1, U52, U18 PC port pins 18~25
4. Check cable connecting keyboard and main PCB.
5. Check keyboard PCB.
6. Check key switches.

Does lock key LED light?

1. Check connector connections.
2. Check lock key control output.
   (1) U39
   (2) U18 PC port pin 11

⑥

No loading from cassette

1. Check connections with cassette tape recorder.
2. Check connecting cable.
3. Computer internal check
   (1) J8 check
       Pin 5
   (2) CMT input circuit check
       U48, C6, C7, R7~R14

No saving onto cassette

1. Check connections with cassette tape recorder.
2. Check connecting cable.
3. Computer internal check
   (1) J8 check
   Pin 4
   (2) CMT output circuit check
   R25, R26, R30, C71
   (3) PPI check
   U18 PC port pin 12

No remote control

1. Check connections with cassette tape recorder.
2. Check connecting cable.
3. Computer internal check
   (1) J8 check
   Pins 6, 7
   (2) CMT remote control circuit check
   R29, TR2, D6, RY1
   (3) PPI check
   U18 PC port pin 13

⑦

Joystick check

1. Check the connecting connectors.
   J3, J4
2. Computer internal check
   (1) General-purpose output circuit check
   (2) PSG input/output port check
   Input ports: IOA0~IOA5
   Output ports: IOB0~IOB6

⑧

1. Check connections with printer.
2. Check connecting cable.
3. Computer internal check
   (1) J5 check
   (2) Printer control circuit check
   U2, U29, U25
   (3) I/O decoder circuit check
   U22, U41, U44, U45

⑨

Read through the above section on troubleshooting and re-check.

III. CIRCUITRY DESCRIPTION

This unit uses a Z-80A CPU, an 8255 PPI and a 4864 RAM. If you are unfamiliar with these LSI chips, it is recommended that you read the introductory guide to these LSI first. Similarly, this section includes some details on the PSG (programmable sound generator: YM2149) and VDP (video display processor: TMS9929A) but reference should be made to the LSI introductory guide for more information. The circuitry description is divided into 10 sections:

* Block diagram
* CPU
* Memory
* I/O ports
* PPI and keyboard
* PSG and joystick interface
* VDP
* Cassette interface
* Printer interface
* Power supply circuits

III-1. BLOCK DIAGRAM

Fig. III-1 is a block diagram of this unit. It indicates that the unit is composed of the following four main LSI chips:

* CPU (central processing unit)
* PPI (programmable peripheral interface)
* VDP (video display processor)
* PSG (programmable sound generator)

The PPI is an LSI with three 8-bit ports and the input/output mode of these ports is switched by requests from the CPU. The VDP has a 16K V-RAM and it controls the character display and graphic display. This LSI outputs the video composite signal which is modulated by the RF modulator on the main PCB to provide the RF output signal. The PSG has three independent oscillators and sounds can be produced by specifying their oscillation frequencies, envelopes and sound levels using software. Apart from its sound functions, this LSI has two 8-bit input/output ports which are used for controlling the two joysticks and reading data stored on cassette. The transmission of data to the keyboard, slot selection and to the cassette and the remote control mode are all controlled by the PPI, and the printer interface is controlled directly when addressed from the CPU. The ROM is a masked 32K ROM which contains BASIC and BIOS. The RAM is 64K-byte of type 4864 dynamic RAM and it is refreshed by the CPU. The unit also uses two cartridge slots, and games can be played by loading ROM cartridges into the slots.

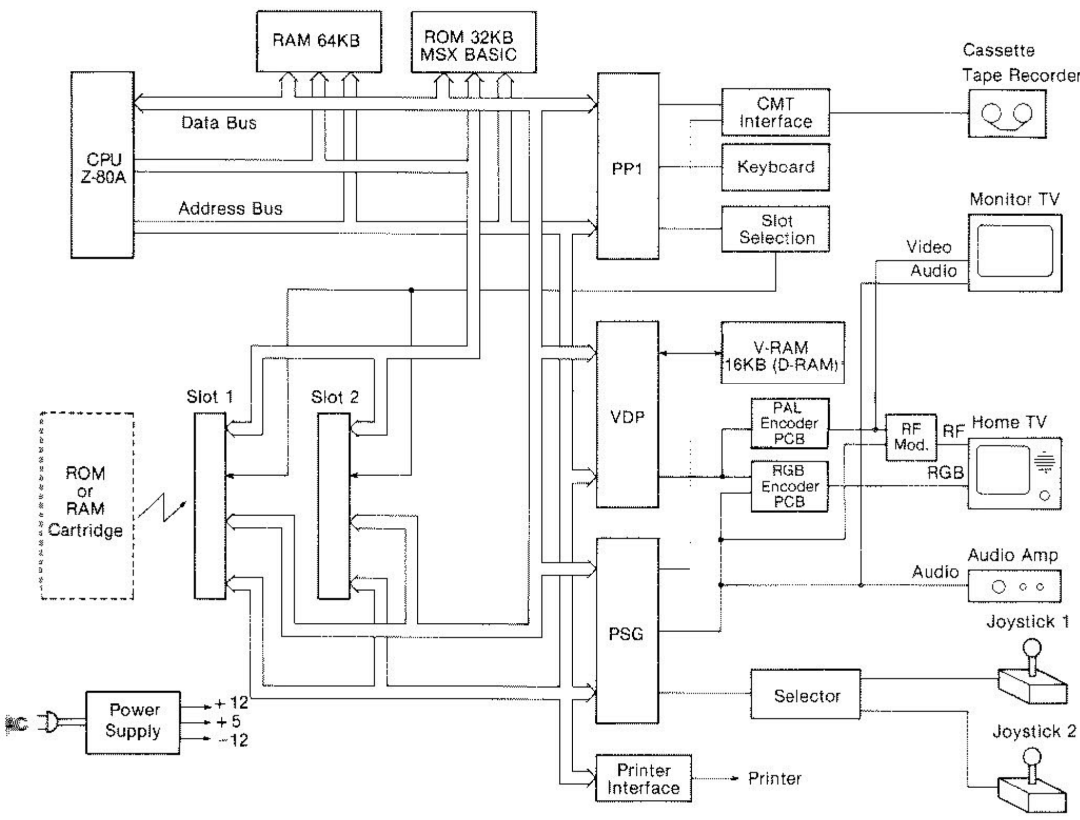


Fig. III-1

III-2. CPU

A high-speed Z-80A or its equivalent is used for the CPU. Its main signals are described below.

CLOCK (ϕ)

The frequency of the OSC block is counted down to onefourth (3.579545 MHz) by the U49 2-stage flip-flop, its rise characteristics are enhanced by the U2 inverter and the signal is finally connected to the CPU.

$\overline{\text{RESET}}$

The CPU and LSI $\overline{\text{RESET}}$ and RESET signals are produced by the reset circuit composed of TR3, U41 and other parts. After the +5V voltage rise occurring when the unit's power is switched on is delayed by the C36 charging, TR3 turns on and the RESET signal is then inverted by U41 for use. D5 in this circuit is used to speed up the C36 discharging when the power is switched off.

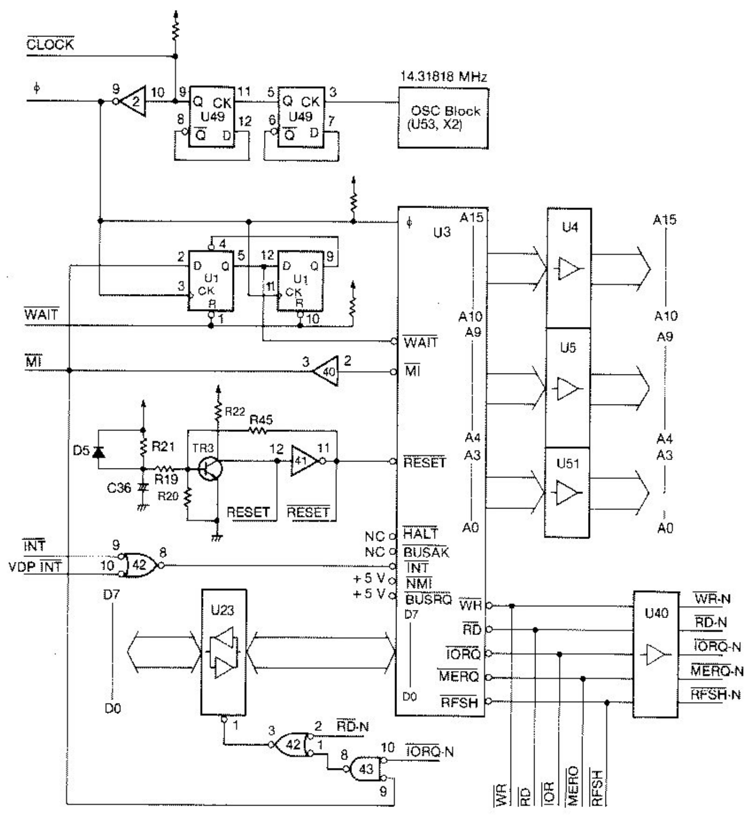


Fig. III-2

$\overline{\text{WAIT}}$

In accordance with the MSX standard, a wait cycle is inserted after the CPU M1 cycle by the U1 flip-flop. When the CPU fetches the command OP code, the M1 signal is set low. This low signal which has passed through U40 resets the first stage U1 at the next CLOCK signal rise edge and this Q pin low signal is input to the CPU $\overline{\text{WAIT}}$ pin.
By resetting the second stage U1 at the next CLOCK signal rise edge, the first stage U1 is set directly and the $\overline{\text{WAIT}}$ pin is set high.
The $\overline{\text{WAIT}}$ signal from the cartridge slots is input into the CPU by directly resetting the first stage U1.

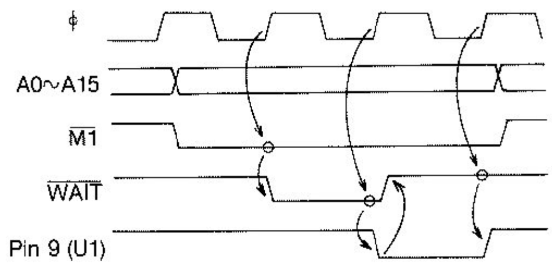


Fig. III-3

$\overline{\text{INT}}$

Mode 1 is used for interrupts with MSX BASIC. The interrupt generated every 1/50 sec. from the VDP and the interrupt from the cartridge slot are OR-ed at U42 and connected to the CPU. Only the $\overline{\text{INT}}$ interrupt signal is used with this unit; the $\overline{\text{NMI}}$ signal is not used.

$\overline{\text{HALT}}$, $\overline{\text{NMI}}$, $\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$

These signals are not used with this unit.

System control signals ($\overline{\text{M1}}$, $\overline{\text{RFSH}}$, $\overline{\text{MERQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$)

In order to satisfy the MSX standard fan-out, the system control signals are connected to the cartridge slots and devices through the U40 driver. In areas of the main PCB where gate delays pose problems, they are used directly without passing through the driver.

Address bus signals (A0~A15)

As with the system control signals, the address bus signals are connected to the cartridge slots and devices through the U4, U51 and U5 drivers.

Data bus signals (D0~D7)

Since a bidirectional data bus is used, the data bus signals are connected to the cartridge slots and devices through the U23 transceiver.

With normal I/O and memory operation the signals are input when the $\overline{RD}$ signal is low and output when the $\overline{WR}$ signal is low. When the mode 2 interrupt is designated by an external ROM or machine language, the vector must be read without the $\overline{RD}$ signal from I/O after the interrupt signal ($\overline{INT}$ = low) has been received. A gate is configured by U42 and U43 to resolve this.

The vector after the interrupt is sent from I/O to the CPU when the $\overline{IORQ}$ and $\overline{M1}$ signals have been set low after the CPU has received the $\overline{INT}$ signal.

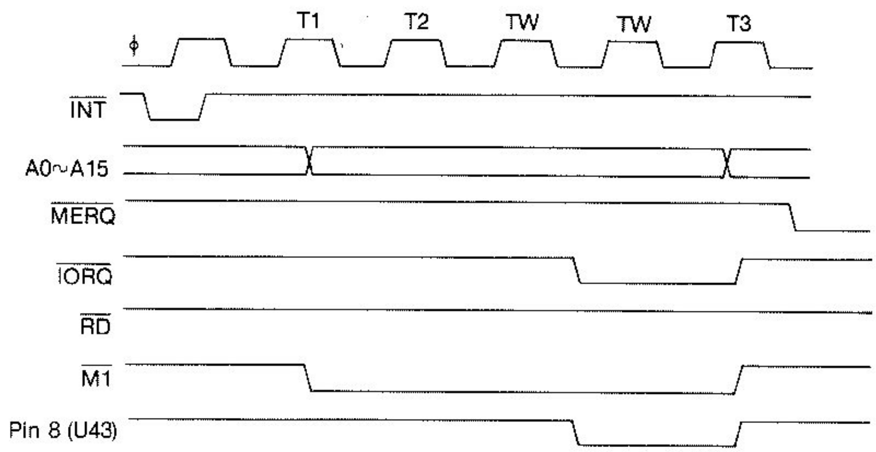


Fig. III-4

III-3. MEMORY

A 32 K masked ROM (HM613256) and 64 K dynamic RAM are mounted on the unit's main PCB while it is also possible to provide memories in 16K units for each of the slots with MSX BASIC support.
These memories are selected and arranged at each slot by writing the data into the PPI ports with software.

Memory map
As shown in Fig. III-5, the MSX memory space is selected and arranged in page units of 16 K, produced by dividing 64 K by four.
On the main PCB the 32 K ROM is accommodated in slot 0 and the 64 K RAM in slot 3. The remainings slots 1 and 2 are similarly arranged in 16 K page units. However, with MSX BASIC the system RAM can be accommodated only in the area above address 8000H.
For BASIC the largest RAM area which is mounted continuously from the FFFF address to the 8000 address is made to serve as the system RAM area.

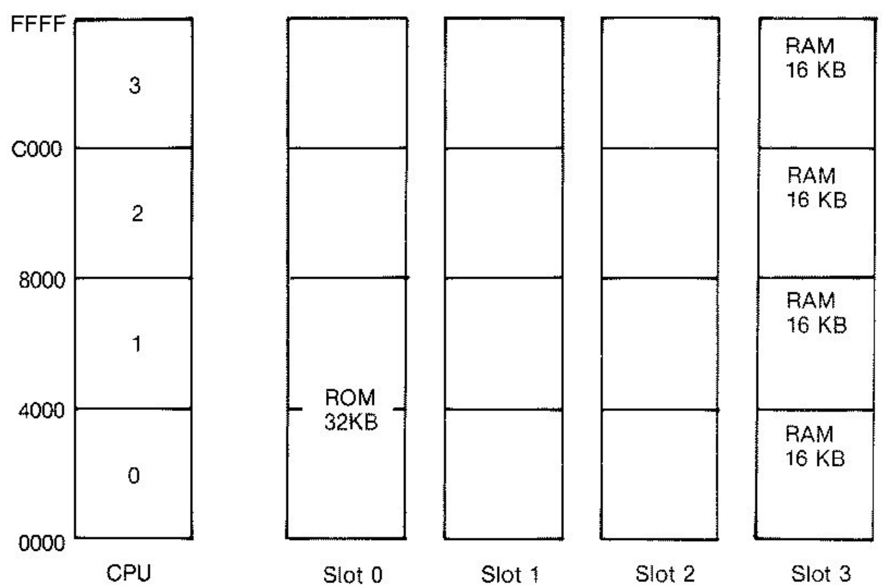


Fig. III-5

Slot selection

Under the MSX standard, the memory space is divided into slots of 64 K each and each slot is further divided into 16 K page units.

When the system is initialized after the power has been switched on, a check is conducted on the pages of each slot to see whether memories are mounted. If required, the slots are selected page by page. This is controlled by the slot selection circuit which is composed of U16 and U17. The U18 (PPI) PA port is a register which stores the slots for each page and its bit configuration is shown in Table III-1.

Bit	Configuration
PA0/PA1	These designate the slot of the 0000~3FFF address page
PA2/PA3	These designate the slot of the 4000~7FFF address page
PA4/PA5	These designate the slot of the 8000~BFFF address page
PA6/PA7	These designate the slot of the C000~FFFF address page

Table III-1

The table clearly shows that two bits designate the slot for each page and so actually 4 slots can be designated for each page.

Fig. III-6 shows the unit's slot selection circuit. The data received from the PPI PA0-PA7 ports are divided into page unit slot select signals by U17 with the A14 and A15 address bus high-order 2 bits, these signals are decoded by U16 and slot select signals $\overline{\text{SLTSL0}}$, $\overline{\text{SLTSL1}}$, $\overline{\text{SLTSL2}}$ and $\overline{\text{SLTSL3}}$ are produced. The $\overline{\text{SLTSL0}}$ signal is used as the enable signal of only the ROM on the main PCB. The unit's RAM is accommodated in logical terms in slot 3 and so the $\overline{\text{SLTSL3}}$ signal is used as its enable signal. The signals which have NAND-ed the $\overline{\text{MERQ}}$ and $\overline{\text{RFSH}}$ signals are connected so that the slot select signals are not output to the U16 $\overline{\text{G}}$ pin (15) when the D-RAM is refreshed.

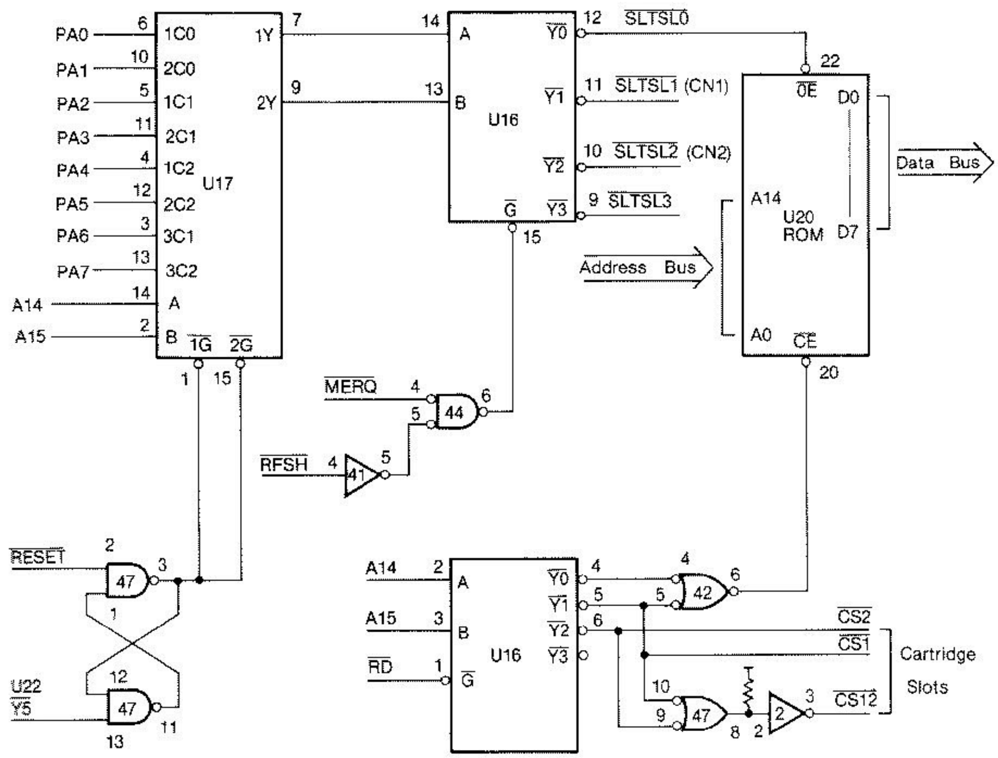


Fig. III-6

ROM select signals

Apart from the slot select signals, it is stipulated that the ROM select signals listed below be output to the cartridge slots. Therefore, these signals are produced at U2, U47 and U16 using the address bus high-order 2 bits and $\overline{RD}$ signal. (Refer to Fig. III-6.)

When the 4000-BFFF address ROM cartridge is used, the advantage is that the cost of the cartridge itself can be reduced since the address decoder circuit is located in the main unit.

Signal	Details
CS1	ROM 4000~7FFF address select signal
CS2	ROM 8000~ address select signal
CS12	ROM 4000~BFFF address select signal (for 256 K ROM)

Table III-2

D-RAM access

Eight type 4864 64K D-RAMs are used in this unit as the system RAM. Besides its usual read/write capacity, the D-RAM is characterized by the fact that its memory operation must be executed for each of the 256 row addresses within 2 msec. because of the way it is constructed. This operation is known as «refreshing.»

The Z-80A CPU contains the circuitry required for refresh control and refreshing is performed once every time each step of the command is executed.

Fig. III-7 shows the D-RAM control circuitry and Fig. III-8 the timing for normal memory access (no refreshing). When the CPU accesses the memory, the desired memory address is first placed on the address bus. Next, the CPU sets the $\overline{MERQ}$ signal low at the T1 clock signal rise. This signal enables the U16 slot select signal. The shaded areas in the timing chart denotes gate delays. This low signal passes through U42 and U44 and it sets the D-RAM $\overline{RAS}$ pin to low, and the D-RAM reads the address bus low-order 8 bits as the row address. U25 is then reset at the down of the next clock signal, the D-RAM $\overline{CAS}$ pin is set low and the address bus high-order 8 bits are read as the column address. The address bus row and column addresses are selected by the U6 and U7 selectors using the U41 and U43 gate delays and the $\overline{RAS}$ signal. For refreshing, the CPU first places the refresh address on the address bus and it then sets the $\overline{RFSH}$ and $\overline{MERQ}$ signals low, these signals are gated by U42 and U44 and the $\overline{RAS}$ pin is set low.

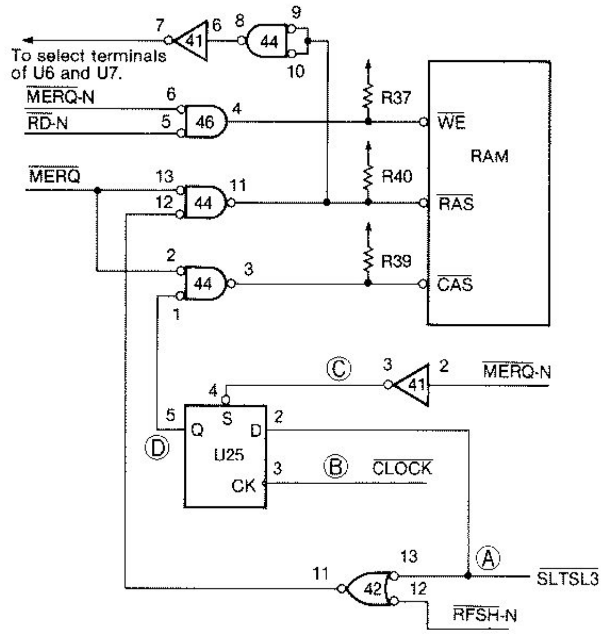


Fig. III-7

Memory Read Cycle

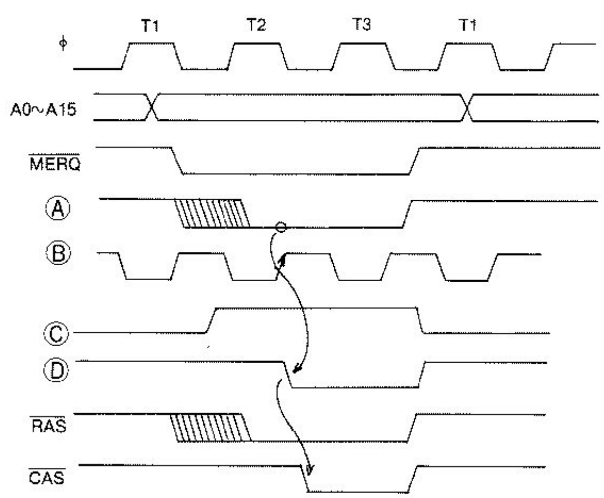
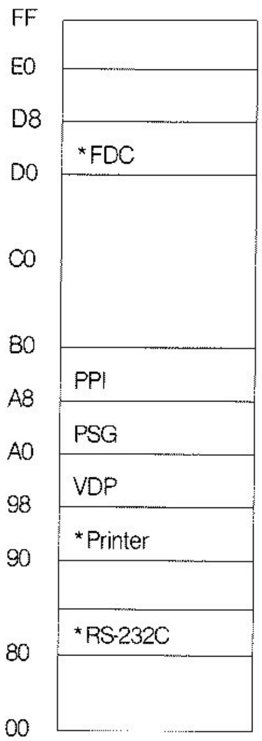


Fig. III-8

III-4. I/O PORTS

The Z-80A employs the $\overline{IORQ}$ signal and the low-order 8 bits (A0~A7) of the address bus and it enables the I/O ports to be connected from the 00H to the FFH addresses.
Under the MSX standard, addresses 80H~FFH are used by the system.
When the address bus A6 is set low and A7 is set high by the U22 decoder, A3, A4 and A5 are decoded and the various I/O select signals are produced. The $\overline{M1}$ signal is connected to the enable pin E1 so that the I/O cannot be selected by the $\overline{IORQ}$ signal produced by the CPU when a mode 2 interrupt is received. The 00H-7FH address I/O ports are not used with this unit.
Table III-3 lists the addresses and their functions.



I/O ADR	RW	Function	Remarks
&H98	W	Data write in V-RAM	9929A
	R	Data read from V-RAM	
&H99	W	Command, address setting	
	R	Status read	
&HA0	W	Address latch	YM2149
&HA1	W	Data write	
&HA2	R	Data read	
&HAB	W	Port A data write	8255
	R	read	
&HA9	W	Port B data write	
	R	read	
&HAA	W	Port C data write	
	R	read	
&HAB	W	Mode setting	
&H90	W	Strobe output (b0)	Latch output
	R	Status input (b1)	BUSY "1"
&H91	W	Print data	Latch output

As indicated in the table, I/O addresses 80 to FF are for system use. Empty columns denote system reserves.
Addresses 00 to 7F can be used as desired but since the same addresses have been allotted between different systems, it may not be possible to use the addresses simultaneously. Basically, I/O devices should be placed in the memory space.

Table III-3

III-5. PPI AND KEYBOARD

"PPI" stands for programmable peripheral interface. It has three 8-bit ports (PA, PB, PC) and the bits of the PC port can be divided into the high-order 4 bits and low-order 4 bits by mode control from the CPU. Although there are 3 modes (0, 1, 2), mode 0 in which the PPI is used as a simple I/O port is designated in this unit.

The PPI is basically used as follows. Before the data are transferred, the mode and port IN/OUT setting data are written into the PPI with the A0 pin high, A1 pin high and WR pin low.

Then, as shown in Table III-4, the port and data transfer is conducted by combining the A0, A1, $\overline{RD}$ and $\overline{WR}$ pin signals. Table III-5 shows the PPI's bit allocation and Fig. III-9 shows the keyboard layout.

A1	A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	0	1	Data bus ← Port PA
0	1	0	1	Data bus ← Port PB
1	0	0	1	Data bus ← Port PC
0	0	1	0	Port PA ← Data bus
0	1	1	0	Port PB ← Data bus
1	0	1	0	Port PC ← Data bus
1	1	1	0	Mode, port IN/OUT setting

Table III-4

PPI bit allocation

Port	Bit	I/O	Signal	Function
A	0 1	O	CS0L CS0H	0000~3FFF address slot designation signal
	2 3		CS1L CS1H	4000~7FFF address slot designation signal
	4 5		CS2L CS2H	8000~BFFF address slot designation signal
	6 7		CS3L CS3H	0000~FFFF address slot designation signal
B	0 ~ 7	I		Keyboard return signal
C	0 1 2 3	O	KB0 KB1 KB2 KB3	Keyboard scan signal
	4		CASON	Cassette control (L = ON)
	5		CASW	Cassette write signal
	6		CAPS	CAPS lamp signal (lights when low)
	7		SOUND	Sound output with software

Table III-5

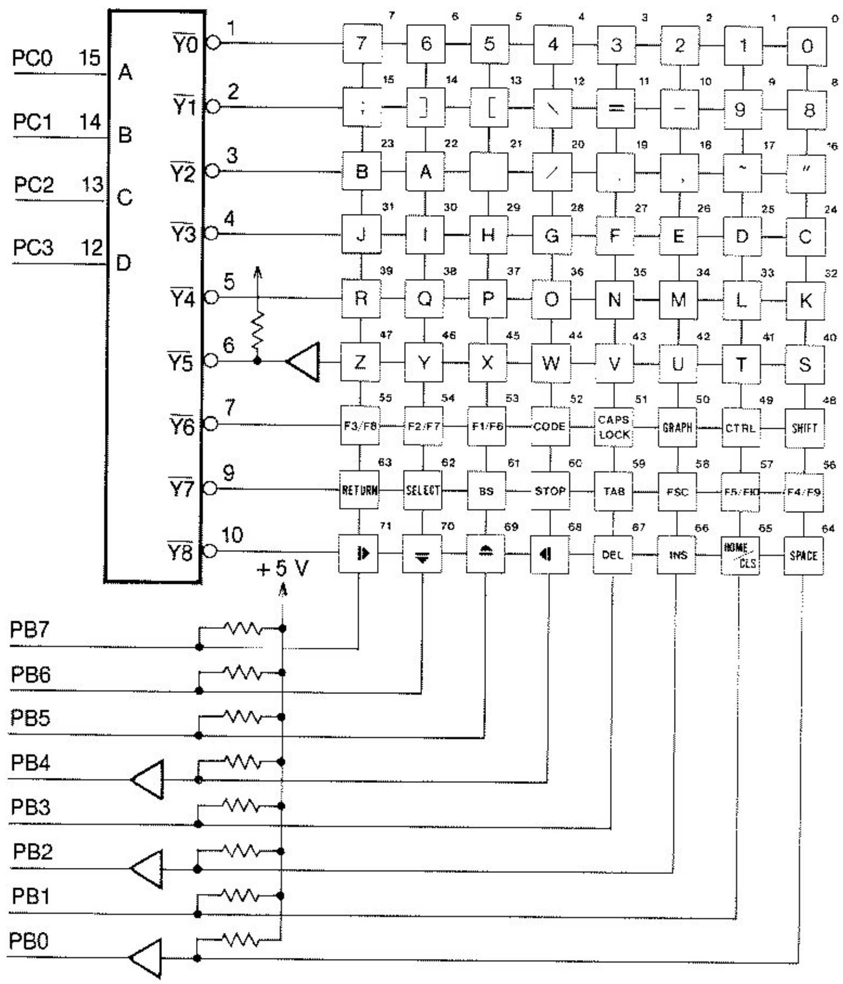


Fig. III-9

Note:

Keyboard layout in this illustration is applicable for the UK version. For the French version, refer to part VII in this book.

III-6. PSG AND JOYSTICK INTERFACE

"PSG" stands for programmable sound generator. Fig. III-10 gives its logical internal structure and register functions.

Operating principle

Inside the PSG are 16 8-bit registers from R0 to R15, of which R0 to R13 control the sound directly and R14 and R15 are used as I/O ports for general purposes.

Also inside the PSG are three frequency-variable oscillators, a noise generator and a low-frequency oscillator for controlling the envelope pattern. Their frequencies are determined by the contents of the corresponding registers. The sound produced by the 3 oscillators and noise generator is mixed for each of the oscillators by a mixer, the volume is controlled by attenuators A, B and C, and the sound is output. It is also possible to produce a fluctuating howling sound by varying the attenuators in accordance with the envelope generator pattern in the cycle generated by the low-frequency oscillator.

The average frequency (fHz) of the A, B and C oscillators and of the noise generator can be designated by converting the value of D found from the formula below in binary and by entering it into the registers.

$$D = 1789772.5/16 \times fHz \fallingdotseq 11860/fHz$$

Similarly, the frequency of the low-frequency oscillator can be sought from the formula below:

$$D = 1789772.5/256 \times fHz \fallingdotseq 6991/fHz$$

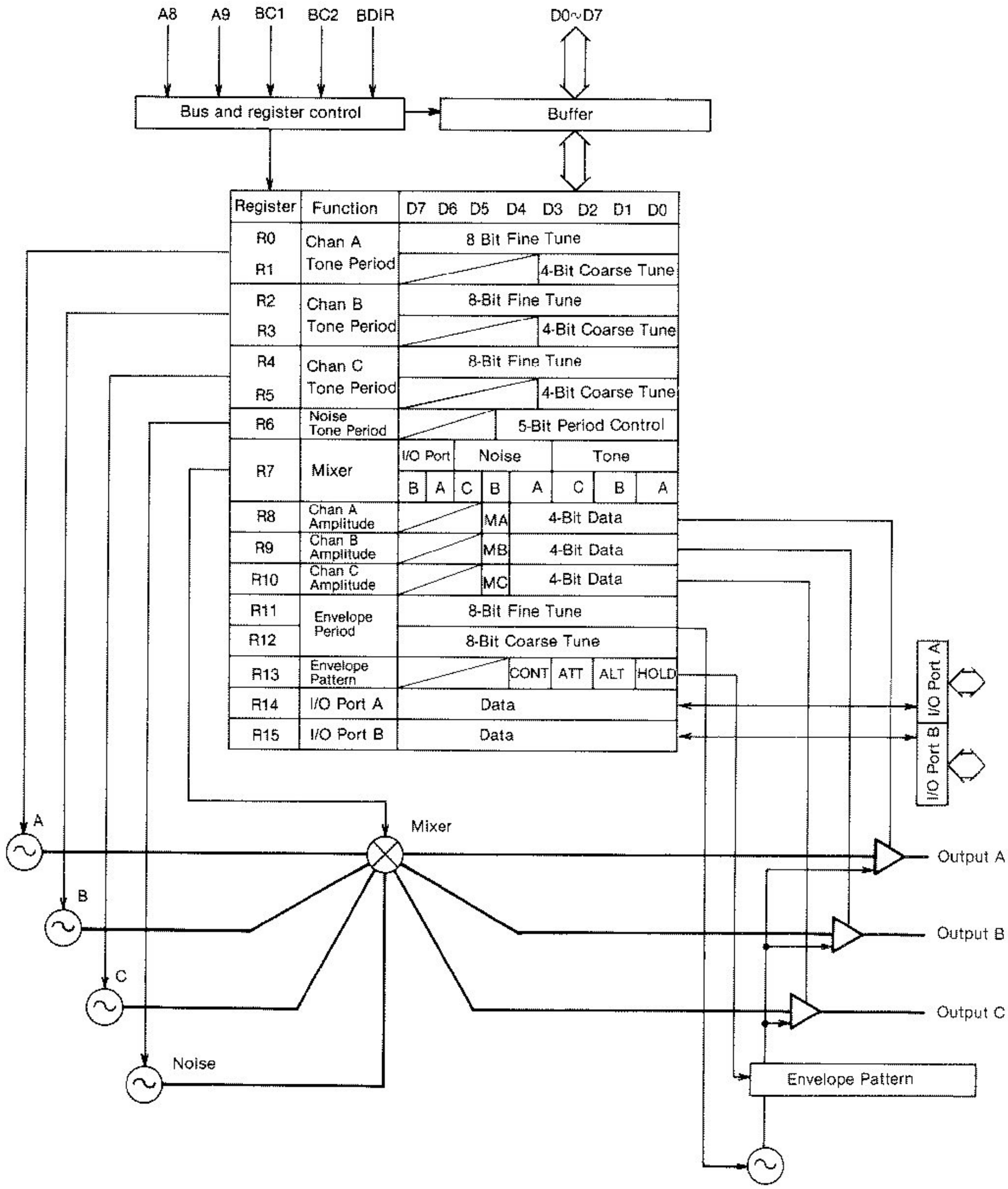

A8
A9
BC1
BC2
BDIR
D0~D7
Bus and register control
Buffer
Register
Function
D7 D6 D5 D4 D3 D2 D1 D0
R0
R1
Chan A
Tone Period
8 Bit Fine Tune
4-Bit Coarse Tune
R2
R3
Chan B
Tone Period
8-Bit Fine Tune
4-Bit Coarse Tune
R4
R5
Chan C
Tone Period
8-Bit Fine Tune
4-Bit Coarse Tune
R6
Noise
Tone Period
5-Bit Period Control
R7
Mixer
I/O Port
Noise
Tone
B A C B A C B A
R8
Chan A
Amplitude
MA
4-Bit Data
R9
Chan B
Amplitude
MB
4-Bit Data
R10
Chan C
Amplitude
MC
4-Bit Data
R11
R12
Envelope
Period
8-Bit Fine Tune
8-Bit Coarse Tune
R13
Envelope
Pattern
CONT
ATT
ALT
HOLD
R14
I/O Port A
Data
R15
I/O Port B
Data
I/O Port A
I/O Port B
A
B
C
Noise
Mixer
Output A
Output B
Output C
Envelope Pattern

Fig. III-10

PSG access

The PSG is accessed by the CPU which operates the BC1 and BDIR pins. Table III-6 gives the BC1 and BDIR pin combinations and functions.

BC1	BDIR	Function
0	0	Places PSG data bus in high-impedance state
1	0	CPU reads contents of register connected to data bus
0	1	CPU writes data into register connected to data bus
1	1	Designates register connected to data bus

Table III-6

Fig. III-11 shows the PSG select circuit and Fig. III-12 is the circuit's timing chart.

When the CPU selects the I/O, the desired I/O address is placed on the address bus, and the $\overline{IORQ}$ and $\overline{RD}$ or $\overline{WR}$ signals are set low. Since the U43 pin 1 is the output of I/O address decoder U22, it is set low after a slight delay from the $\overline{IORQ}$ signal down, and if the U43 pin 2 Ⓕ is low, the U46 gate is enabled and the BC1 and BDIR signals are output corresponding to address buses A0 and A1. Furthermore, the Ⓐ low signal is inverted by U41 and Ⓓ terminal of the first stage U21 is set high. Consequently, the first stage U21 is set at the Ⓓ signal rise. The Ⓓ clock signal is the reversed $\overline{CLOCK}$ signal and so is in phase with the CPU's basic clock ϕ signal. In other words, Ⓒ is set high at the Tw rise. The second stage U21 is set at the rise of the next ϕ signal and Ⓔ is set low. When the $\overline{CLOCK}$ signal is high, that is, when ϕ is low after Ⓔ is set low, the U46 gate condition is satisfied and Ⓕ is set high. Ⓖ is also set high and BC1 and BDIR are set low.

The Ⓐ signal is enabled by the $\overline{IORQ}$ signal and so when the $\overline{IORQ}$ signal is high, U41 is inverted, Ⓑ is set low, the U21 flip flop is directly reset and Ⓒ is set low and Ⓔ high.

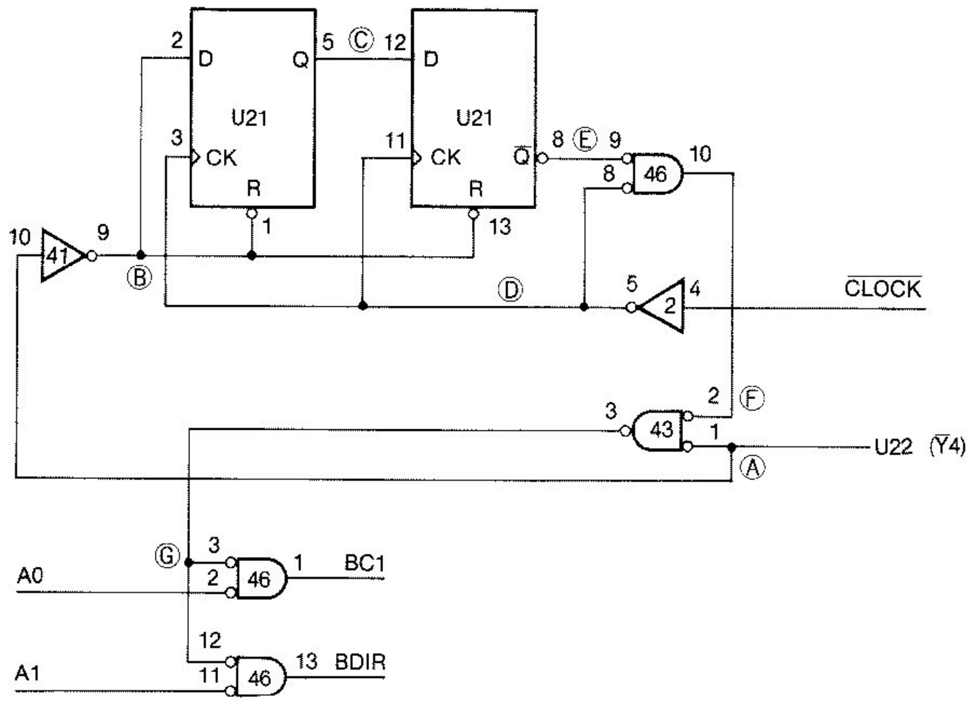


Fig. III-11

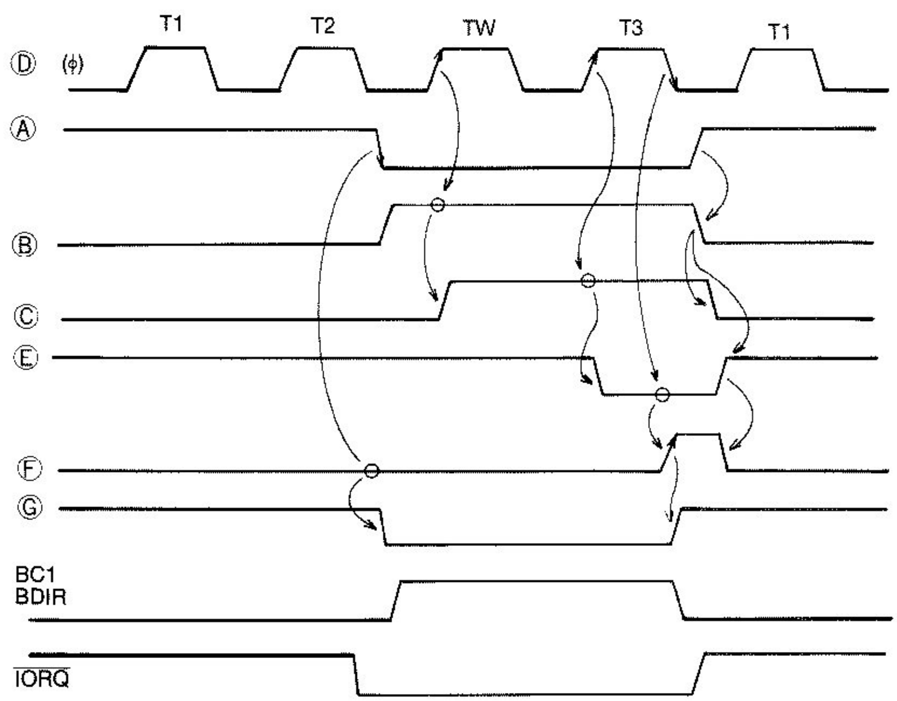


Fig. III-12

I/O Ports

Inside the PSG are two 8-bit ports, port A and port B. The input/outputs are determined by controlling bits 6 and 7 of the register R7. Table III-7 gives the combinations and functions of bits 6 and 7 of register 7. In this unit port A is used as an input and port B as an output.

Bit 7	Bit 6	Port A	Port B
0	0	Input	Input
0	1	Input	Output
1	0	Output	Input
1	1	Output	Output

Table III-7

Table III-8 gives the PSG bit allocation and Fig. III-13 shows the flow of the signals when the joystick is used.

PSG bit allocation

Port	Bit	I/O	Connector pin		Signal when joystick is used
A	0	I	J3-1	*1	FWD1
			J4-1	*2	FWD2
	1		J3-2	*1	BACK1
			J4-2	*2	BACK2
	2		J3-3	*1	LEFT1
			J4-3	*2	LEFT2
	3		J3-4	*1	RIGHT1
			J4-4	*2	RIGHT2
	4		J3-6	*1	TRGA1
			J4-6	*2	TRGA2
	5		J3-7	*1	TRGB1
			J4-7	*2	TRGB2
	6		Key layout designation input (Connect to +5 V)		
	7		CSAR (cassette tape read)		
B	0	O	J3-6	*3	High level
	1		J3-7	*3	High level
	2		J3-6	*3	High level
	3		J4-7	*3	High level
	4		J3-8		
	5		J4-8		
	6		Port A input select		
	7		Not used		

Table III-8

1. Effective when bit 6 of port B is low. For joystick 1.
2. Effective when bit 6 of port B is high. For joystick 2.
3. These pins should be set high when they are not used as output ports. Signals are output through open collector buffers.

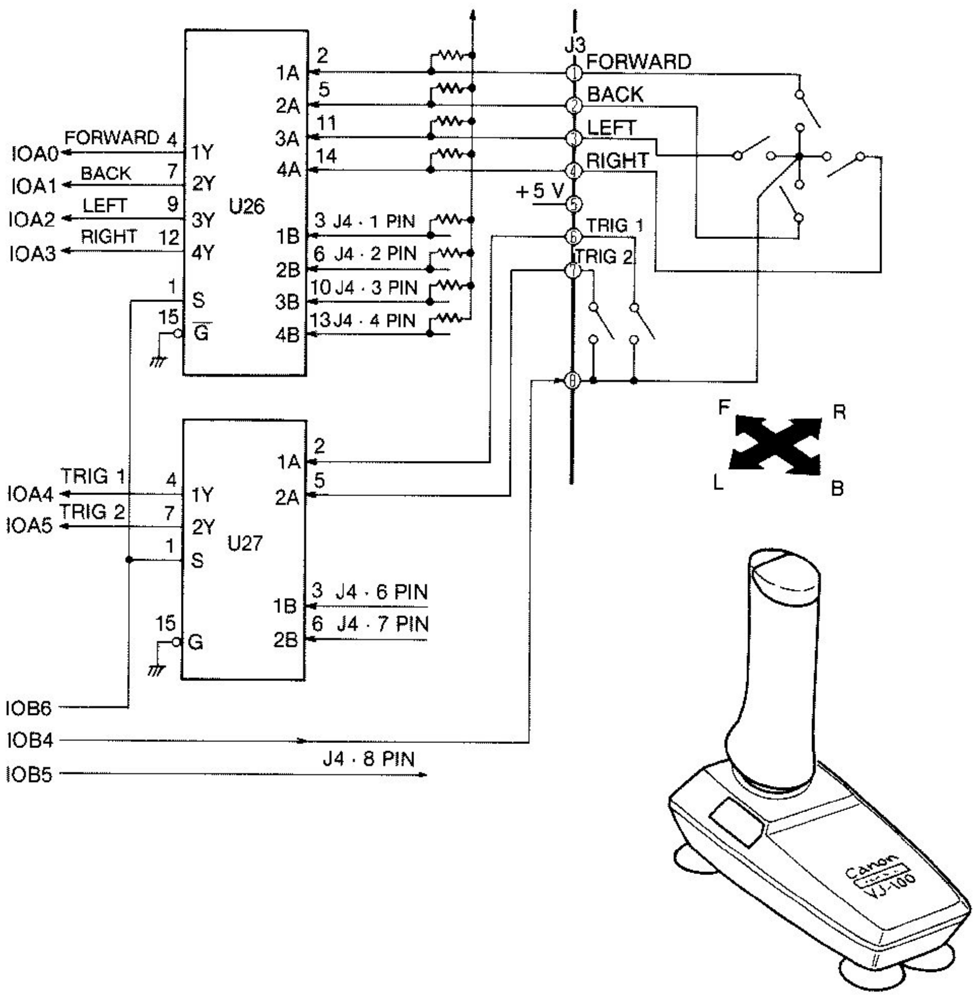

U26
U27
J3
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
S
G
IOA0
IOA1
IOA2
IOA3
IOA4
IOA5
IOB6
IOB4
IOB5
FORWARD
BACK
LEFT
RIGHT
TRIG 1
TRIG 2
+5 V
J4 · 1 PIN
J4 · 2 PIN
J4 · 3 PIN
J4 · 4 PIN
J4 · 6 PIN
J4 · 7 PIN
J4 · 8 PIN
F
R
L
B
Canon
VJ-100

Fig. III-13

III-7. VDP

VDP is an abbreviation of Video Display Processor; this single IC performs all controls pertaining to the Display. The VDP used is the TMS9929A produced by Texas Instruments, and is equipped with graphics display of 192 x 256 elements, 32 surface sprite surface function convenieint for games and animation, 16 colour simultaneous display, and a V-RAM refresh function. The VDP outputs three colour signals, R-Y, Y, and B-Y.
The VDP contains 8 internal write only registers and 1 internal read only status register, plus an external 16 k-byte V-RAM, and thus controls the screen in accordance with the data from these devices. The following is an explication of the image signal processing for the UK and French versions.

UK version

In the UK version, the VDP's colour difference signal output R-Y, Y, B-Y signals are sent to the PAL encoder circuit board, where they are converted into a video composite signal in confirmity with PAL-I. The desired image is produced on the TV screen as the electron beam is swept in the horizontal and vertical directions, and specific colours are specified.
The horizontal sweep is performed in 64 μsec from left to right, and the vertical sweep is performed from top to bottom in about 20 msec. Namely, 312 horizontal sweeps occur in the period of a single vertical sweep. However, with actual TV sets, the beginning timing of the vertical sweep is offset by the time of one vertical sweep, so that 313 horizontal sweeps are inserted, thus giving the screen greater detail. This is called an interlacing system, but this system is not used on the present IC.
In Fig. III-14, the part indicated by the broken line is the inserted horizontal sweep. A single horizontal sweep signal is composed of a horizontal sync signal, a colour burst signal, and a video (image) signal. The horizontal sync signal is for the purpose of timing the horizontal sweep. The colour burst signal is a 4.43 MHz burst signal, and has the function of synchronizing the phase of the colour sub-carrier oscillator within the TV. And the 4.43 MHz frequency component of the following video signal has its phase compared and detected with the colour sub-carrier oscillator, and the colour signal is thus produced. However, with the PAL-system, the phase of the colour burst is alternately changed between +135° and +225° every other horizontal sweep. This is in order to reduce phase distortion produced in the transmission line.
The amplitude of the AC component within the video signal expresses colour tone, and the DC level of the average amplitude value expresses colour depth.
Each vertical sweep is composed of 312 horizontal sweeps, and at the head of each such sweep, a vertical sweep syc signal is impressed in order to time the vertical sweep.
The PAL encoder circuit board produces the video composite signal from the R-Y, Y, B-Y signals. This composite signal passes through the rear panel video out connector and is supplied to the monitor TV, while at the same time it is modulated at the UHF 36 channel frequency (591.25 MHz) by the RF modulator, and passing through the rear panel RF connector, it is supplied to the TV set's antenna terminal. In addition, the audio signal from the PSG is also modulated to the radio frequency (597.25 MHz) of the same channel by the RF modulator.

French version

In the French version, the RGB encoder circuit board produces the colour signals R (red), G (green) and B (blue), and the sync signal needed for timing the horizontal and vertical sweeps from the VDP colour difference signal.
Since the Y signal output from the VDP is the luminance signal, it contains a certain fixed ratio α, β, γ of the respective colour signals RGB. Namely,
$Y = \alpha R + \beta G + \gamma B$

Accordingly, if the values of α, β, and γ are known, the G signal can be obtained from the Y, R, and B signals.
The R signal can be obtained from the sum of the R-Y signal and the Y signal thus,
$R = (R - Y) + Y$
In the same way, the B signal can be obtained as the sum of the B-Y and Y signals:
$B = (B - Y) + Y$
In this way, the RGB encoder PCB produces the three primary colour signals R, G, and B from the Y, R-Y, and B-Y signals input from the VDP. Also, the sync signal is produced by slicing the luminance signal Y.

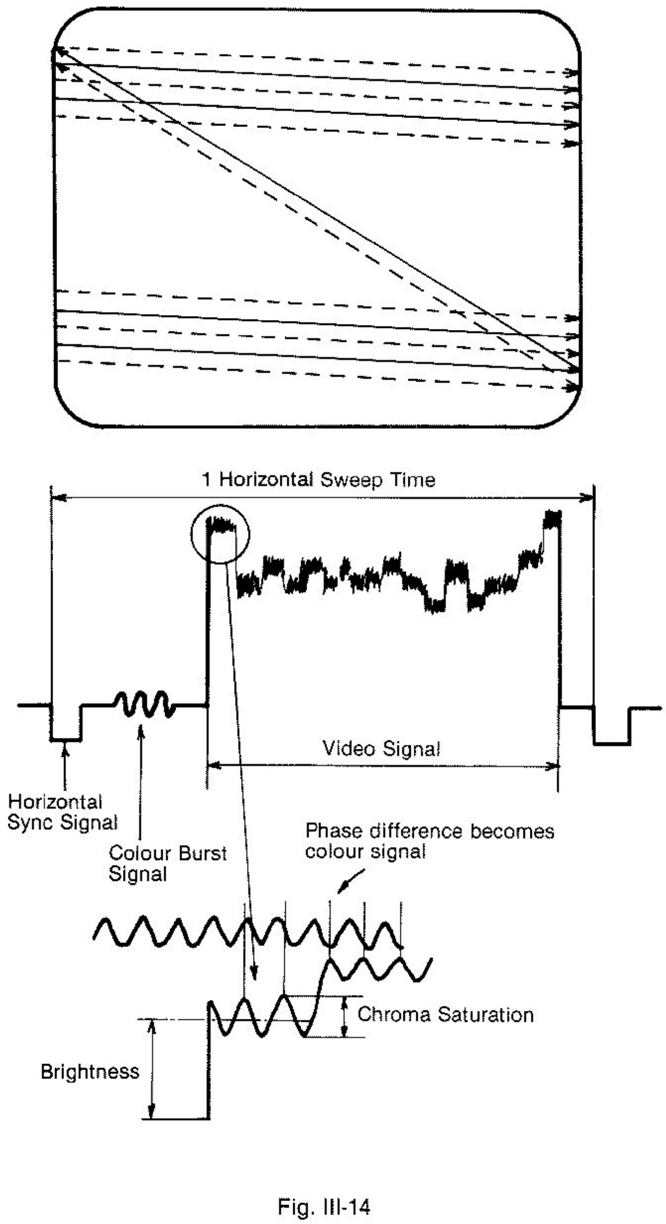


Fig. III-14

Interface

Interface with the CPU is provided by combinations of 3 signals, $\overline{CSW}$, $\overline{CSR}$ and MODE. Access to the VDP can be divided broadly into two ways: read/write of the registers inside the VDP and access of the V-RAM through the VDP.
Table III-9 gives the functions of the 3 control signals.

Signal	Function
MODE	This is set low when data are transferred from the CPU TO THE V-RAM or vice versa. At all other times it is high.
$\overline{CSR}$	When set low, the VDP outputs 8-bit data to the data-bus
$\overline{CSW}$	This is set low when writing 8-bit data from the CPU. The data are set into the VDP with the rise of this signal.

Table III-9

Interface with the CPU is provided by connecting the MODE pin with the A0 signal of the address bus and by connecting the $\overline{CSR}$ and $\overline{CSW}$ pins through the U28 gate. U28 is enabled when the CPU selects 98H and 99H as the I/O addresses and it judges whether data should be transferred to the V-RAM by the A0 signal.

Writing data into the VDP register

Data are written into the VDP register (write-only) as shown in Fig. III-10 for selecting the display mode and other functions and for setting the base address.

		$\overline{CSW}$	$\overline{CSR}$	MODE
1st byte data	D7 D6 D5 D4 D3 D2 D1 D0	Low	High	High
2nd byte data	1 0 0 0 0 RS0 RS1 RS2	Low	High	High

Table III-10

The data to be written are sent first, the D7 bit is set high and registers 0 through 7 are designated by RS0, RS1 and RS2.

Reading data from the VDP status register

The CPU reads out data in bytes from the status register. The control signals are as follows.

		$\overline{\text{CSW}}$	$\overline{\text{CSR}}$	**MODE**
Status register contents	D7 D6 D5 D4 D3 D2 D1 D0	High	Low	High

Table III-11

Writing data into the V-RAM

The CPU transfers data through the VDP to the V-RAM using the 14 bit auto increment address register inside the VDP. Two bytes are required to set the address register.

		$\overline{\text{CSW}}$	$\overline{\text{CSR}}$	**MODE**
1st byte (address set)	A6 A7 A8 A9 A10 A11 A12 A13	Low	High	High
2nd byte (address set)	0 1 A0-A1 A2 A3 A4 A5	Low	High	High
3rd byte (data)	D7 D6 D5 D4 D3 D2 D1 D0	Low	High	Low

Table III-12

The V-RAM's high-order 8 bit address is set with the first byte, bit D7 is set to 0 and bit D6 to 1 and the low-order 6 bit address is set with the second byte, and the write data are sent with the 3rd byte. Once the address register is set, it is automatically incremented and so after this it is acceptable for the data only ($\overline{\text{CSW}}$ low, $\overline{\text{CSR}}$ high, MODE low) to be sent without the address having to be set.

Reading out data from the V-RAM

The procedure for reading data from the V-RAM is, basically, the same as that for writing data. However, there are two differences: when data are read, $\overline{CSR}$ is low and the D6 bit of the second byte is low.

		$\overline{CSW}$	$\overline{CSR}$	MODE
1st byte (address set)	A6 A7 A8 A9 A10 A11 A12 A13	Low	High	High
2nd byte (address set)	0 0 A0 A1 A2 A3 A4 A5	Low	High	High
3rd byte (data)	D7 D6 D5 D4 D3 D2 D1 D0	High	Low	Low

Table III-13

CLOCK

The VDP uses a crystal oscillator to produce the sync, colour burst and video signals required for the picture. Care should be exercised since if this frequency shifts, the picture will be thrown into disarray. The clock signal is adjusted with trimmer capacitor TC1. For details, refer to the section on adjustments in Chapter 2.

V-RAM

Eight type 4116 D-RAMs are mounted for each bit of the registers to serve as the V-RAM. The VDP performs all the V-RAM read/write and refresh timing operations.

III-8. CASSETTE INTERFACE

The cassette interface has remote control functions which control the input and output and cassette recorder motor, and its transmission rate can be set by the program to 1,200 or 2,400 baud.
SK is used as the recording system and with a 1,200-baud rate 2,400 Hz is used for marks and 1,200 Hz for spaces.
When a program is saved on tape, the CPU sends the data to bit 5 of port C and after the data have passed through the R30/C71 integrator circuit, their level is aligned by R25 and R26 and they are output to pin 4 of J8. When a program is loaded from a tape, the sine-wave signals received from pin 5 of J8 are converted into digital signals by the U48 Schmitt circuit and the signals are read into the CPU through bit 7 of the PSG's port A.
The remote control functions are carried out by shorting or opening pins 6 and 7 of J8 using relay contacts. The signals are output from bit 4 of the PPI's port C and TR2 is turned on in the low active state.

III-9. PRINTER INTERFACE

I/O addresses 90H and 91H are used for the printer. When the CPU has selected 90H or 91H as the I/O address, the decoder $\overline{\text{Y2}}$ pin of the U22's address decoder is set low and U45 is enabled. 45 decodes the $\overline{\text{RD}}$-N, $\overline{\text{WR}}$-N and A0 signals, and when A0 is low or, in other words, when $\overline{\text{RD}}$-N is low with 90H, pin $\overline{\text{Y2}}$ is set low, U2 is enabled and the busy signal from the printer is placed on bit 1 (D1) of the data bus. In the same way, when $\overline{\text{WR}}$-N is low, the U25 strobe flip-flop is set at the rise by the data bus bit D0.
When A0 is high and $\overline{\text{WR}}$-N is low, pin $\overline{\text{Y5}}$ is set low and the printing data are set in U29 at the rise. Table III-15 shows the timing with the printer.

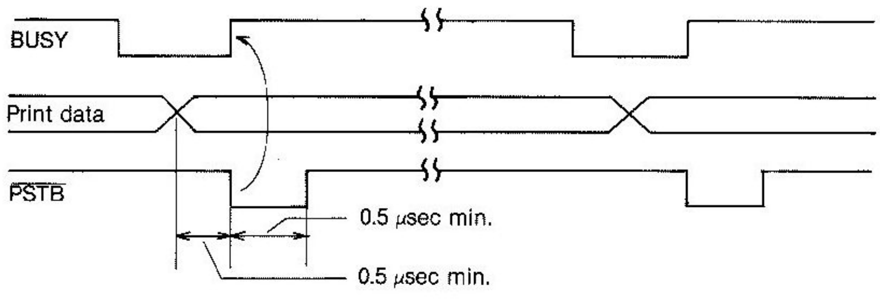


Fig. III-15

III-10. POWER SUPPLY CIRCUITRY

This unit provides a +5 V voltage for the logic ICs, +5 V, −5 V and +12 V voltages for the D-RAMs and also a −12 V voltage for the cartridge slots and operational amplifier used for the audio output.
The power PCB produces the +5 V, +12 V and −12 V voltages while the −12 V voltage is produced by regulating the −5 V voltage with zener diode D4 on the main PCB.

+5 V

An AC voltage of about 11 V is input from the primary of the power transformer across pins 5 and 4 of CN1, this is rectified by diode bridges D1, D2, D3 and D4 to a DC voltage of about 12 V and it is then input into a regulator IC. U1 is a chopper regulator.
Zener diode ZD1 for generating the reference voltage is connected to pin 3 and the reference voltage is adjusted by VR1.
TR1 connected to pin 4 is for detecting overcurrents. When an overcurrent is detected with a drop in the voltage of R4, TR1 is turned on and pin 4 is set low, and the oscillator circuit inside the IC stops and no longer outputs a signal.
Fig. III-16 indicates the circuitry inside the U1.

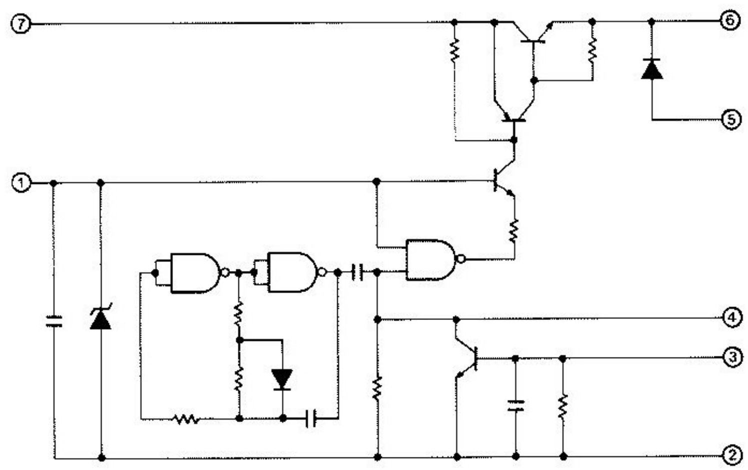


Fig. III-16

+12 V

An AC voltage of about 14 V is supplied from the secondary of the power transformer across pins 2 and 3 of CN1, this is rectified by diode bridge D5 to a DC voltage of about 19 V and it is then input into regulator IC U2. Resistor 8 across pins 1 and 3 of this IC is a bypass resistor which reduces the load on the regulator.

−12 V

An AC voltage of about 14 V is supplied from the secondary of the power transformer across pins 2 and 3 of CN1, this is rectified by diode bridge D5 to a DC voltage of about −19 V and it is then input into regulator IC U3.

III-11. TEST PROGRAM

A PROM-based diagnostic program is available for testing the unit's basic functions.

Booting up the test program

The test program is stored on a PROM (type 2764) and so the cartridge with this PROM is inserted into cartridge slot 2 and the program starts to run automatically when the power is switched on. This happens so that when the system is initialized after the power has been switched on, the slot statuses are checked and control is automatically transferred to the ROM when a ROM has been inserted in one of the slots. This ROM uses address 8000H to 9FFFH.

* When conducting the test with a printer or other peripheral connected, first switch on the unit's power and then switch on the peripheral's power. Upon completion of the test, first switch off the peripheral's power and then switch off the unit's power.
* The test program used is different for different versions. Be sure to check the number marked on the ROM cartridge.

UK: TKC-0480-000
French: TKC-0481-000

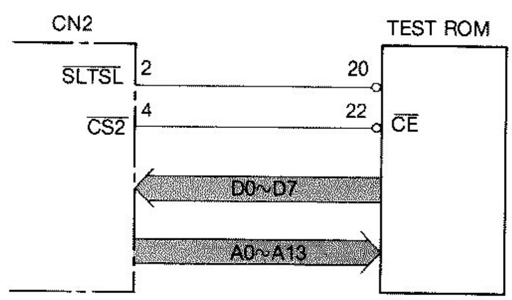
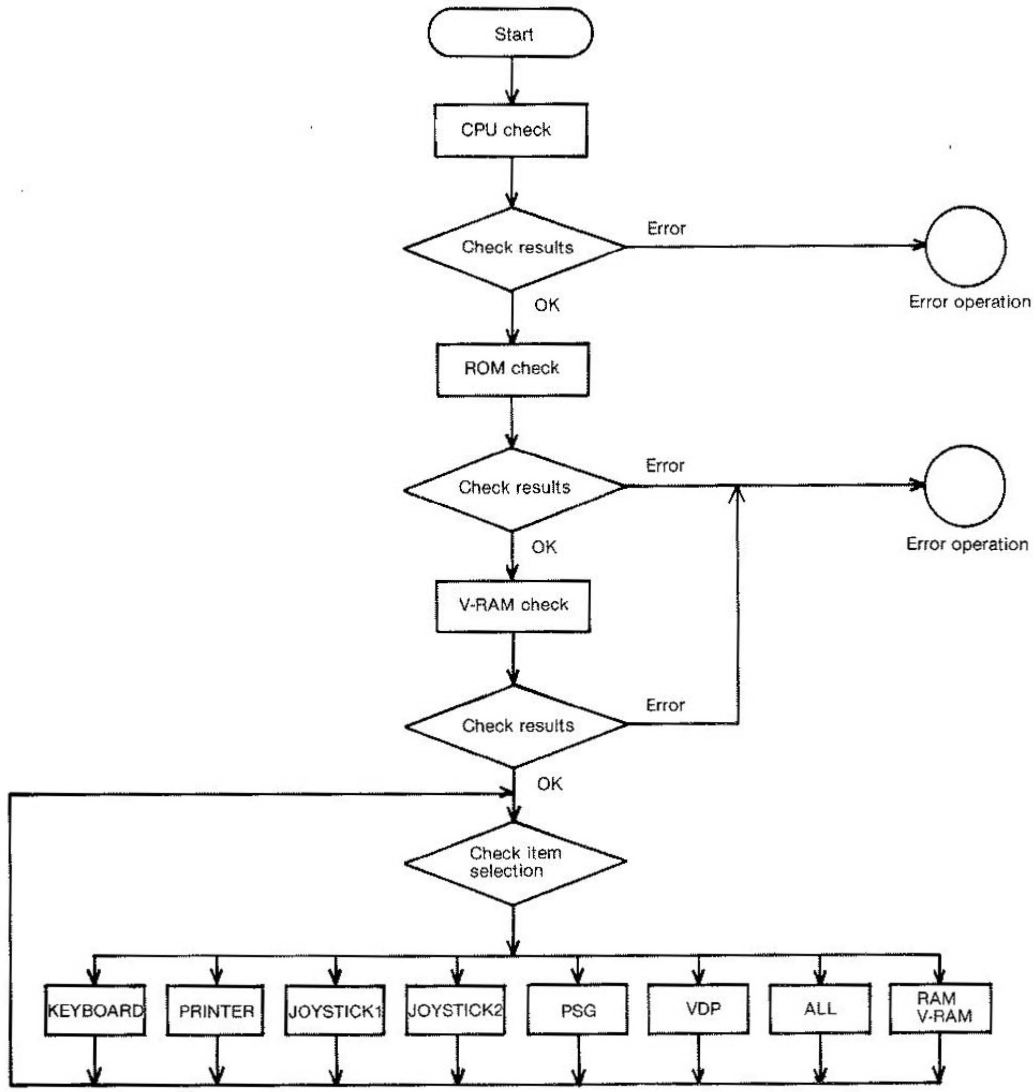


Fig. III-17

Flow chart

A flow chart of this test program is shown below. The CPU test, ROM test and V-RAM test are conducted before the menu screen appears and if no errors are detected, the menu screen is then displayed.

The desired test can be conducted after the menu screen appears by entering numbers 0 to 7.



CPU test

Details:	This test conducts a read/write check for all the Z-80A's registers and also executes the conditional jump commands where the flags are set and reset.
Completion:	Proceed to the next ROM test when the "CPU Check OK!!" message appears.
Error:	The program loops after the "CPU NG!!" message appears. To escape from the loop, switch the power off and then start again.

32 K ROM test

Details:	This test performs an exclusive-OR operation one byte at a time for the MSX BASIC ROM from address 0000 to address 7FFF and it compares the results with the regular data.
Completion:	Proceed to the next test when the "ROM Check OK!!" message appears.
Error:	"The ROM NG AA/BB" message appears. AA denotes the data of the regular ROM exclusive-OR-ed results and BB the data of the ROM in which the error has occurred. Operation can be moved on to the next test when the [ESC] key is punched.

V-RAM test

Details:	This test writes and verifies the reading of all the inverted data among the data stored from address 0000 to address 3FFF of the V-RAM and then it writes and verifies the reading of the original data before inversion.
Completion:	The "V-RAM Check OK!!" message appears and the menu screen is displayed.
Error:	The "V-RAM NG!! XXXX AA/BB" message appears. XXXX denotes the hexadecimal address where the error has occurred, AA the data which have been written and BB the data which have been read. To continue testing, press the [ESC] key.

Menu

The menu screen is displayed when the CPU, ROM and V-RAM tests have been completed without any errors discovered. When numbers 0 to 7 are typed in accordance with the display, the selected program is started.

Keyboard test

Details: This test checks all the keys and the upper-case LED. As soon as this program starts, the upper-case LED lights.
The key input order is as described below. If the wrong keys are punched, the key which should be punched is indicated on the screen along with a beep.

Completion: The "If test is OK, then type [RETURN] key." message appears.
Operation returns to the main menu when the [RETURN] key is punched.

Error: If the wrong key is punched, the proper key is indicated up to 3 times on the screen along with a beep. If the correct key is not punched when displayed for the fourth time, the "If you type [ESC] key, then return MENU." display appears along with a beep.
When the ESC key is now punched, the "If test is OK, then type [RETURN] key." message appears and operation returns to the main menu when the [RETURN] key is punched.

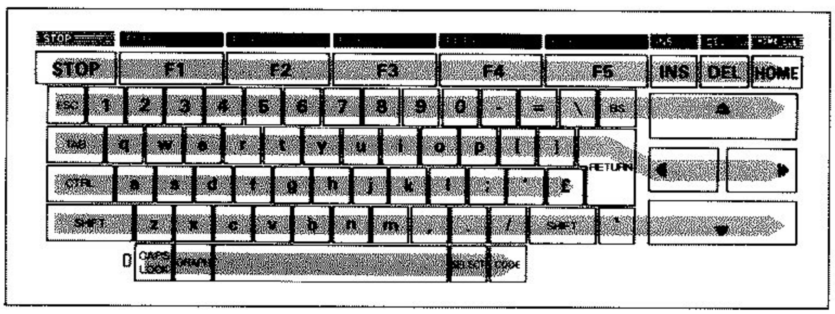


Fig. III-18

Printer test

Details: This first checks that the printer's busy signal is low and then it outputs all the MSX characters. Two line feeds are sent to the printer and this is repeated 8 times. If the busy signal is high from the start, the "Printer is not connected." message appears. To escape, press the [RETURN] key and the completion routine is entered.

Completion: When the test is completed, the "If test is OK, then type [RETURN] key." message appears and a return is made to the main menu by punching the [RETURN] key.

Joystick test (1 or 2)

Details: This test displays the status of the selected joysticks's connector on the screen. When the [RETURN] key is punched, operation moves on to the TRIGGER (A) test. When the trigger A button is punched, "0" is displayed on the screen. The [RETURN] key is punched again in order to complete the TRIGGER (A) test. Operation then moves on to the TRIGGER (B) test. In the same way, the [RETURN] key is punched to complete this test.

Completion: When the "If test is OK, then type [RETURN] key." message appears, a return is made to the main menu as soon as the [RETURN] key is punched.

PSG test

Details: The "do re mi fa so la si do" notes of a single octave are output in the order of the PSG's oscillators A, B, C, A, B, C, A and B.
Next, the "do mi so," " re fa la," "mi so si" and "fa la do" chords are output with the lowest note by oscillator C, the middle note by oscillator B and the highest note by oscillator A.
Finally, the frequency of oscillator A is changed and the "ambulance" sound is mixed with the noise.

Completion: When the "If test is OK, then type [RETURN] key." message appears, a return is made to the main menu as soon as the [RETURN] key is punched.

Error: There is no error message.

VDP test

Details: This test is divided into the 7 sections below. Operation moves on to the next section when the [RETURN] key is punched.

1. Character display in graphic mode 1
2. Colour bar display in graphic mode 2
3. Colour bar display in multi-colour mode
4. Sprite collision on screen
5. Sprite screen 5 is cleared and a 5-colour sprite is displayed
6. Sprite magnification. The display in (5) is magnified 4 times and 16 times each time the [RETURN] key is punched.
7. The sprite displayed in (6) is moved horizontally.

Completion: When section (7) of the test is completed and the [RETURN] key is punched once, the screen is cleared and the "If test is OK, then type [RETURN] key." message appears. A return is made to the main menu when the [RETURN] key is punched.

Error: The following error messages are valid for test sections (4), (5) and (7) only.

4. If the sprite collision cannot be detected, "Collision NG!!" appears. In cases like this, press the [ESC] key to move on to the next test.
5. When an error arises, "Sprite No5 NG!!" appears. In cases like this, press the [ESC] key to move on to the next test.
7. When an error arises, "Sprite moving test NG!!" appears. In cases like this, press the [ESC] key to move on to the end routine.

ALL

Details: When this test is selected, the keyboard, printer, joystick 1, joystick 2, PSG and VDP tests are chained together in sequence and executed. The error messages are as mentioned above under the individual tests.

RAM-V-RAM test

Details: Since the RAM is in slot 3 and the diagnostic program is in addresses 8000-BFFF of slot 2, this test divides the RAM into four segments and performs the following checks in the order below.

1. RAM check of addresses C000-FFFF in slot 3
2. RAM check of addresses 0000-3FFF in slot 3
3. The test now moves the RAM check routine of the diagnostic program in addresses 8000-BFFF in slot 2 to addresses 0000 3FFF in slot 3.
4. RAM check of addresses 8000-BFFF in slot 3.
5. A jump is made to the V-RAM test after the slots are returned to their original status.

Completion: The "RAM Check OK!!" message appears and operation moves on to the next V-RAM test. If the V-RAM test is OK, the "V-RAM Check OK!!" message appears and a return is made to the menu screen.

Error: "RAM NG!! XXXX AA/BB" appears.
XXXX denotes the hexadecimal address where the error has occurred, AA the data which have been written and BB the data which have been read. To continue testing, press the [ESC] key and move onto the next V-RAM test.
For details of V-RAM test errors, refer to the V-RAM test section.

IV. CONNECTOR PIN DESCRIPTION

IV-1. CONNECTOR PIN CONFIGURATIONS

Listing of connectors

The unit is provided with the following I/O connectors:

Connector	Specifications
Video output (UK version)	RCA 2-pin connector
Video/audio output (French version)	DIN 8-pin connector, DIN-45326
Cassette	DIN 8-pin connector, DIN-45326
Joystick connector	AMP 9-pin connector
Cartridge bus	2.54 mm pitch, 50-pin connector
Audio output (UK version)	RCA 2-pin connector
Printer	Amphenol 14-pin connector

Table IV-1

Cassette interface

Input	Connected to earphone jack on cassette recorder
Output	Connected to mic jack on cassette recorder
Sync system	Start/stop sync (asynchronous) system
Transmission	1,200 baud (1,200 Hz, 1 frequency "0", 2,400 Hz, 2 rate frequencies "1") default 2,400 baud (2,400 Hz, 1 frequency "0", 4,800 Hz, 2 frequencies "1") software-selected (2,400 baud usable only with data recorder)
Modulation	FSK system
Remote control	Available
Connector	DIN 8-pin connector

Signals

Pin No.	Signal
1	GND
2	GND
3	GND
4	CMTOUT
5	CMTIN
6	REM+
7	REM−
8	GND

Table IV-2

Pin No. Signal/Pin connections

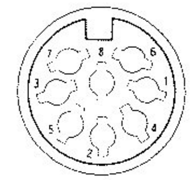


Fig. IV-1

General-purpose I/O port (joystick connector)

IC	YM-2149
I/O	4-bit input, 1-bit output, 2-bit bidirectional (per port)
Logic	Positive
Level	TTL
Connector	AMP 9-pin connector

Signals

Pin No.	Signal
1	FWD
2	BACK
3	LEFT
4	RIGHT
5	+5V
6	TRG 1
7	TRG 2
8	OUTPUT
9	GND

Table IV-3

Pin No. Signal/ Pin connections

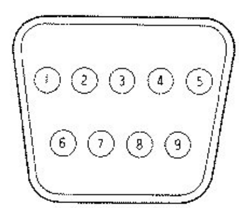
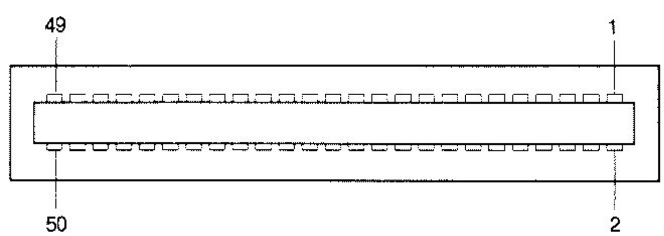


Fig. IV-2

Cartridge bus pin assignments

Pin No.	Signal	I/O*	Pin No.	Signal	I/O*
1	$\overline{\mathrm{CS1}}$	O	2	$\overline{\mathrm{CS2}}$	O
3	$\overline{\mathrm{CS12}}$	O	4	$\overline{\mathrm{SLTSL}}$	O
5	Reserved (Note 1)	—	6	$\overline{\mathrm{RFSH}}$	O
7	$\overline{\mathrm{WAIT}}$ (Note 2)	I	8	$\overline{\mathrm{INT}}$ (Note 2)	I
9	$\overline{\mathrm{M1}}$	O	10	$\overline{\mathrm{BUSDIR}}$	I
11	$\overline{\mathrm{IORQ}}$	O	12	$\overline{\mathrm{MERQ}}$	O
13	$\overline{\mathrm{WR}}$	O	14	$\overline{\mathrm{RD}}$	O
15	$\overline{\mathrm{RESET}}$	O	16	Reserved (Note 1)	—
17	A9	O	18	A15	O
19	A11	O	20	A10	O
21	A7	O	22	A6	O
23	A12	O	24	A8	O
25	A14	O	26	A13	O
27	A1	O	28	A0	O
29	A3	O	30	A2	O
31	A5	O	32	A4	O
33	D1	I/O	34	D0	I/O
35	D3	I/O	36	D2	I/O
37	D5	I/O	38	D4	I/O
39	D7	I/O	40	D6	I/O
41	GND	—	42	CLOCK	O
43	GND	—	44	SW1	—
45	+5 V	—	46	SW2	—
47	+5 V	—	48	+12 V	—
49	SUNDIN	I	50	−12 V	—

*: Signal direction with respect to main unit



Note 1: Reserved pins must not be used.
Note 2: Open-collector output.

Cartridge bus signals

Pin No.	Pin	Description
1	$\overline{CS1}$	ROM 4000-7FFF address slect signal
2	$\overline{CS2}$	ROM 80000-BFFF address select signal
3	$\overline{CS12}$	RPM 4000-BFFF address select signal
4	$\overline{SLTSL}$	Slot select signal. For each slot, the inherent slot select signal is supplied.
5	Spare	Spare pin for future use. Not to be used
6	$\overline{RFSH}$	Refresh cycle signal
7	$\overline{WAIT}$	CPU wait request signal
8	$\overline{INT}$	CPU interrupt request signal
9	$\overline{M1}$	Signal indicating CPU fetch cycle
10	$\overline{BUSDIR}$	External data bus buffer direction control signal. Cartridge is selected and a low signal is output from all cartridges excluding memories with the timing by which the data are sent. Not used with this unit.
11	$\overline{IORQ}$	I/O request signal
12	$\overline{MERQ}$	Memory request signal
13	$\overline{WR}$	Write timing signal
14	$\overline{RD}$	Read timing signal
15	$\overline{RESET}$	System reset signal
16	Spare	Spare pin for future use. Not to be used.
17∼32	A0∼A15	Address bus signal
33∼40	D0∼D7	Data bus signal
41	GND	Signal ground
42	CLOCK	CPU clock 3.579545 MHz signal
43	GND	Signal ground
44, 46	SW1, SW2	For protection when removing and replacing. Not used with this unit.
45, 47	+5 V	+5 V power supply
48	+12 V	+12 V power supply
49	SUNDIN	Sound input signal (−5 dBm)
50	−12 V	−12 V power supply

Table IV-5

Printer interface

Specifications	8-bit level. Handshake with busy and strobe signals
Level	TTL
JIS code standard	
Connector	Amphenol 14-pin (female on unit)
Signals	

Pin No.	Signal	Pin No.	Signal
1	PSTB	8	PDB6
2	PDB0	9	PDB7
3	PDB1	10	NC
4	PDB2	11	BUSY
5	PDB3	12	NC
6	PDB4	13	NC
7	PDB5	14	GND

Table IV-6

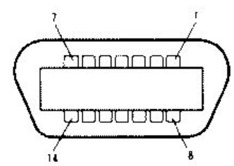


Fig. IV-4

Video/audio output (French version only)

Pin No.	Signal
1	FIRST
2	GND
3	B (BLUE)
4	SYNC
5	R (RED)
6	SLOW
7	AUDIO
8	G (GREEN)

Pin No. Signal/Pin connection

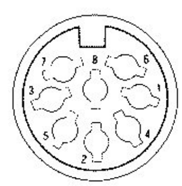
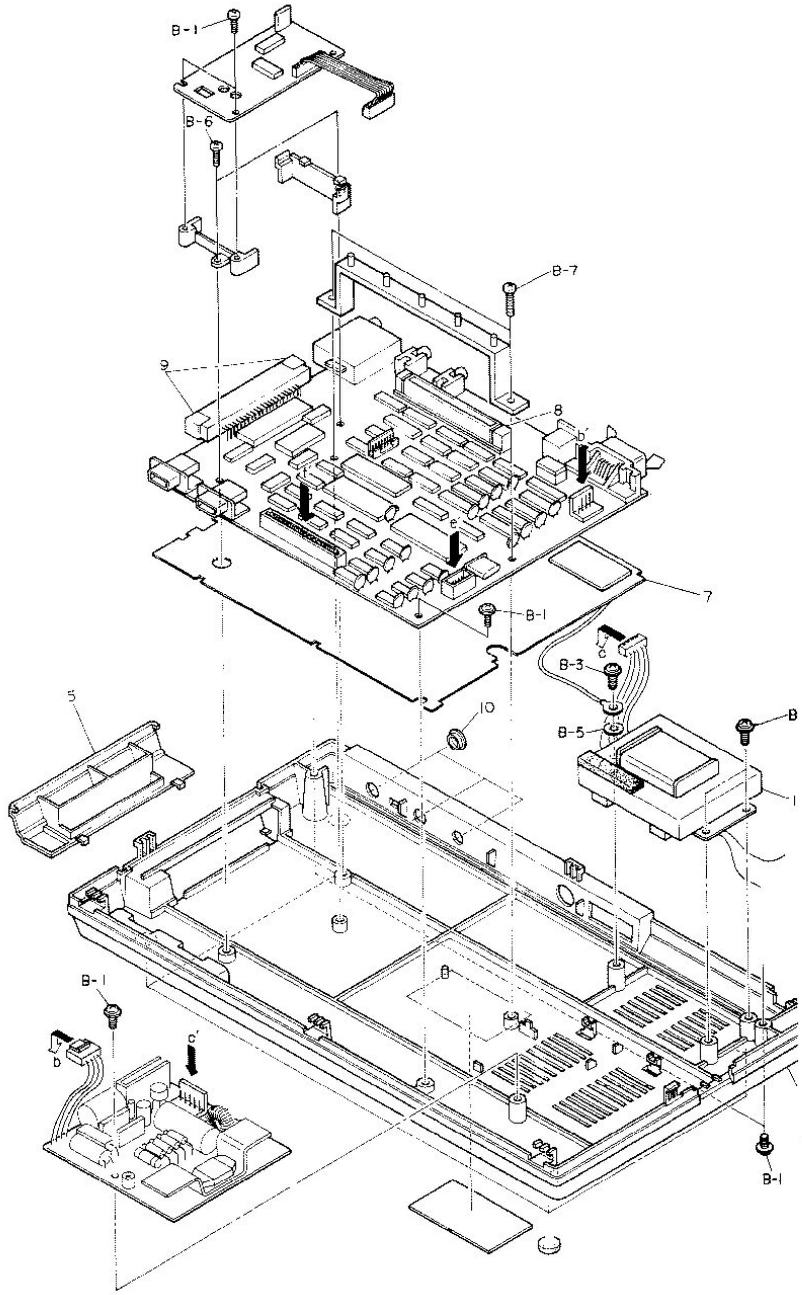


Fig IV-5

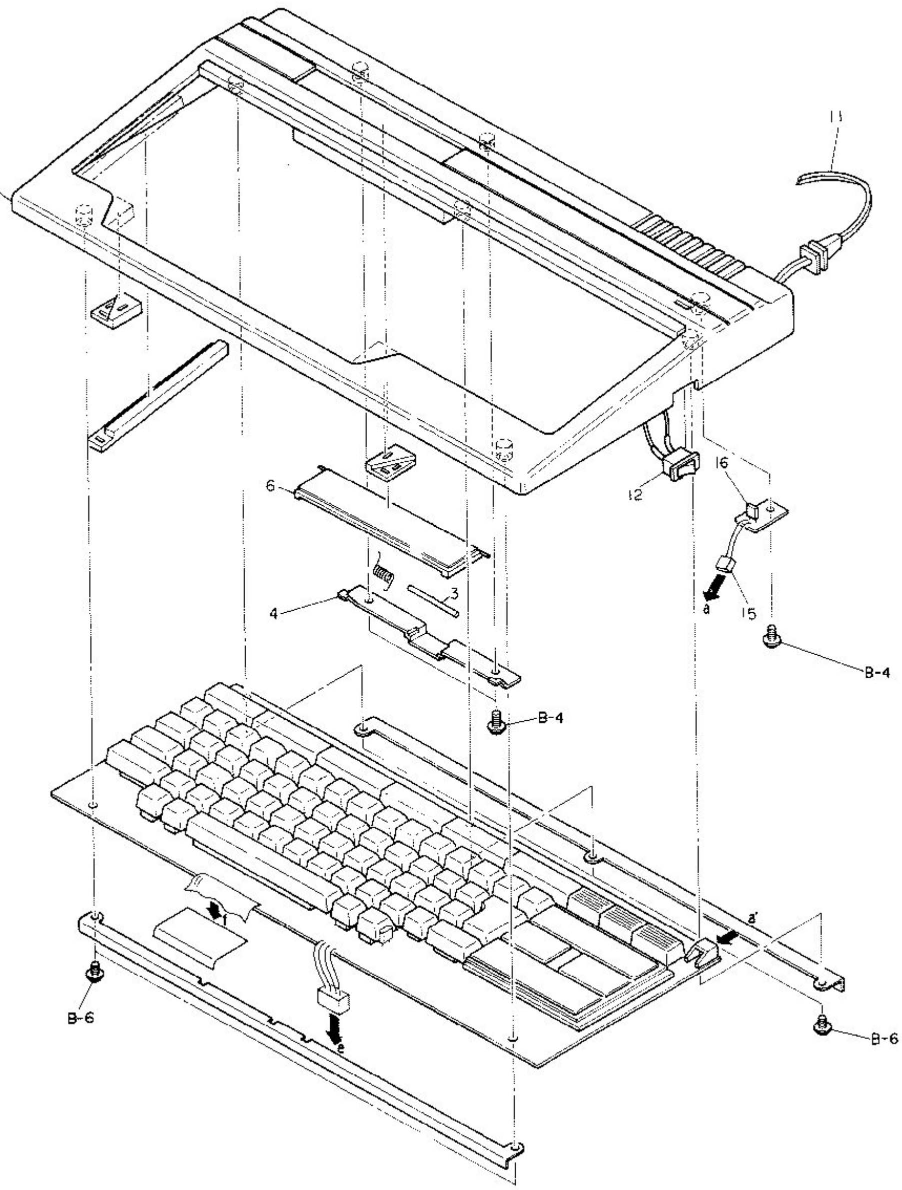
V. ASSEMBLY DIAGRAMS AND PARTS LIST

V-1. EXPLODED VIEW



-3

3



2

V-2. MAIN PARTS

Key	Parts No.	Q'ty	Description	Remarks
1	EY7-0971-000	1	TOP PANEL ASSY.....[FRENCH]	AMMS5***01
	EY7-1091-000	1	.....[UK]	AMMS6***01
2	EY7-0972-000	1	BOTTOM PANEL ASSY.....[FRENCH]	AMMS5***02
	EY7-1092-000	1	.....[UK]	AMMS6***02
3	EY7-0973-000	1	SHAFT	MT320LJ001
4	EY7-0974-000	1	SPRING	MW141LJ001
5	EY7-1102-000	1	SLOT CAP	VB721SH001
6	EY7-1093-000	1	SLOT COVER	VS738SB001
7	EY7-1090-000	1	SHIELD PLATE ASSY	AMMS3***03
8	EY7-0975-000	1	ROMPACK GUIDE	VB622SB001
9	EY7-0976-000	2	SLOT GUIDE	VQ111SB001
10	EY7-1103-000	1	CONNECTOR CAP.....[FRENCH]	VF122RB002
	EY7-1103-000	3	.....[UK]	VF122RB002
11	EY7-1087-000	1	AC CORD ASSY.....[FRENCH]	ACAC218EEA
	EY7-1088-000	1	.....[UK]	ACAC219BSA
12	EY7-0920-000	1	SEA-SAW SWITCH	SC010112UA
13	EY7-0921-000	1	POWER TRANSFORMER	TPC70E001C
14	EY7-1089-000	1	TERMINAL	YZF2080001
15	EY7-0950-000	1	CONNECTOR CORD ASSY	ACCNH05GEA
16	EY7-0983-000	1	LED, GREEN	QLBLN342GN
B-1	XB3-1300-807	8	SCREW, PAN TAPPING, M3X8	BTPP3008PZ
B-2	XB3-2401-005	1	SCREW, TP TAPPING, M4X10	BTP44010BZ
B-3	XB3-1401-005	3	SCREW, PAN TAPPING, M4X10	BTPP4010PZ
B-4	XB3-2300-607	3	SCREW, TP TAPPING, M3X6	BTP43006BZ
B-5	XD1-4100-402	1	INSIDE TOOTHED WASHER	BWU40855SZ
B-6	XB3-1301-007	7	SCREW, PAN TAPPING, M3X10	BTPP3010PZ
B-7	XB3-1301-207	4	SCREW, PAN TAPPING, M3X12	BTPP3012BZ

V-3. KEYBOARD PARTS

UK version

Key	Parts No.	Q'ty	Description	Remarks
	EY7-0977-000	1	CONNECTOR ASSY	ACCNG77GEA
	EY7-0978-000	4	COIL SPRING, FOR CURSOR KEY	MW252SW001
	EY7-0979-000	1	COIL SPRING, FOR SPACE KEY	MW264SV001
	EY7-0980-000	8	KEY GUIDE, FOR SHIFT,RETURN,FUNCTION	MX422LJ001
	EY7-0981-000	2	KEY GUIDE, FOR CTRL,SHIFT	MX422LJ002
	EY7-0982-000	1	KEY GUIDE, FOR SPACE	MX722LJ001
	EY7-0983-000	1	LED, GREEN	QLBLN342GN
	EY7-0984-000	4	KEY SWITCH, FOR CURSOR	SK0111X07A
	EY7-0985-000	1	KEY SWITCH, FOR SPACE	SK0111X09A
	EY7-0986-000	68	KEY SWITCH	SK0111X12A
	EY7-0987-000	1	KEY TOP ESC	VK122SH250
	EY7-0989-000	1	KEY TOP CAPS	VK122SH252
	EY7-0990-000	1	KEY TOP GRAPH	VK122SH253
	EY7-0991-000	1	KEY TOP SELECT	VK122SH254
	EY7-1042-000	1	KEY TOP 1	VK122SH318
	EY7-1043-000	1	KEY TOP 2	VK122SH319
	EY7-1044-000	1	KEY TOP 3	VK122SH320
	EY7-1045-000	1	KEY TOP 4	VK122SH321
	EY7-1046-000	1	KEY TOP 5	VK122SH322
	EY7-1047-000	1	KEY TOP 6	VK122SH323
	EY7-1048-000	1	KEY TOP 7	VK122SH324
	EY7-1049-000	1	KEY TOP 8	VK122SH325
	EY7-1050-000	1	KEY TOP 9	VK122SH326
	EY7-1051-000	1	KEY TOP 0	VK122SH327
	EY7-1003-000	1	KEY TOP -	VK122SH279
	EY7-1038-000	1	KEY TOP +	VK122SH314
	EY7-1052-000	1	KEY TOP \	VK122SH328
	EY7-1005-000	1	KEY TOP A	VK122SH281
	EY7-1006-000	1	KEY TOP Z	VK122SH282
	EY7-1007-000	1	KEY TOP E	VK122SH283

Key	Parts No.	Q'ty	Description	Remarks
	EY7-1008-000	1	KEY TOP R	VK122SH284
	EY7-1009-000	1	KEY TOP T	VK122SH285
	EY7-1010-000	1	KEY TOP Y	VK122SH286
	EY7-1011-000	1	KEY TOP U	VK122SH287
	EY7-1012-000	1	KEY TOP I	VK122SH288
	EY7-1013-000	1	KEY TOP O	VK122SH289
	EY7-1014-000	1	KEY TOP P	VK122SH290
	EY7-1017-000	1	KEY TOP Q	VK122SH293
	EY7-1018-000	1	KEY TOP S	VK122SH294
	EY7-1019-000	1	KEY TOP D	VK122SH295
	EY7-1020-000	1	KEY TOP F	VK122SH296
	EY7-1021-000	1	KEY TOP G	VK122SH297
	EY7-1022-000	1	KEY TOP H	VK122SH298
	EY7-1023-000	1	KEY TOP J	VK122SH299
	EY7-1024-000	1	KEY TOP K	VK122SH300
	EY7-1025-000	1	KEY TOP L	VK122SH301
	EY7-1026-000	1	KEY TOP M	VK122SH302
	EY7-1029-000	1	KEY TOP W	VK122SH305
	EY7-1030-000	1	KEY TOP X	VK122SH306
	EY7-1031-000	1	KEY TOP C	VK122SH307
	EY7-1032-000	1	KEY TOP V	VK122SH308
	EY7-1033-000	1	KEY TOP B	VK122SH309
	EY7-1034-000	1	KEY TOP N	VK122SH310
	EY7-1053-000	1	KEY TOP {	VK122SH329
	EY7-1054-000	1	KEY TOP }	VK122SH330
	EY7-1055-000	1	KEY TOP :	VK122SH331
	EY7-1056-000	1	KEY TOP "	VK122SH332
	EY7-1057-000	1	KEY TOP ~	VK122SH333
	EY7-1058-000	1	KEY TOP <	VK122SH334
	EY7-1059-000	1	KEY TOP >	VK122SH335

Key	Parts No.	Q'ty	Description	Remarks
	EY7-1060-000	1	KEY TOP /	VK122SH336
	EY7-1061-000	1	KEY TOP ACCENT	VK122SH337
	EY7-0988-000	1	KEY TOP BS	VK122SH251
	EY7-1041-000	1	KEY TOP CODE	VK122SH317
	EY7-1062-000	3	KEY TOP INS, DEL, HOME	VK132SB009
	EY7-1063-000	1	KEY TOP TAB	VK132SH013
	EY7-1065-000	1	KEY TOP STOP	VK142SB004
	EY7-1066-000	1	KEY TOP CTRL	VK142SH006
	EY7-1068-000	1	KEY TOP RETURN	VK142SH008
	EY7-1070-000	2	KEY TOP CURSOR (LEFT, RIGHT)	VK143SH001
	EY7-1071-000	5	KEY TOP FUNCTION	VK152SB001
	EY7-1067-000	1	KEY TOP SHIFT (SMALL)	VK142SH007
	EY7-1072-000	1	KEY TOP SHIFT (LARGE)	VK152SH002
	EY7-1075-000	1	KEY TOP SPACE	VK172SH004
	EY7-1076-000	1	KEY TOP CURSOR (UP)	VK183SH001
	EY7-1077-000	1	KEY TOP CURSOR (DOWN)	VK183SH002
	EY7-1078-000	2	PLASTIC RIVET	VM163VB001
	EY7-1079-000	1	LED SHEET	VS115RB001
	EY7-1080-000	1	HOLDER PLATE, FOR FLAT CABLE	VS616VB002
	EY7-1081-000	1	CURSOR KEY FRAME	VS669SH001
	EY7-1082-000	2	KEY GUIDE HOLDER, FOR SPACE	VU111SB002
	EY7-1083-000	2	KEY GUIDE HOLDER, FOR SHIFT,CTRL	VU311SB001
	EY7-1084-000	8	KEY GUIDE HOLDER, FOR SHFT,RTN,FNCTN	VU411SB001
	EY7-1085-000	1	FLAT CABLE	WC17062AS1
	EY7-1086-000	1	JUNCTION JACK, FOR POWER LED	YJF02S044Z

French version

Key	Parts No.	Q'ty	Description	Remarks
	EY7-0977-000	1	CONNECTOR ASSY	ACCNG77GEA
	EY7-0978-000	4	COIL SPRING, FOR CURSOR KEY	MW252SW001
	EY7-0979-000	1	COIL SPRING, FOR SPACE KEY	MW264SV001
	EY7-0980-000	8	KEY GUIDE, FOR SHIFT,RETURN,FUNCTION	MX422LJ001
	EY7-0981-000	1	KEY GUIDE, FOR SHIFT	MX422LJ002
	EY7-0982-000	1	KEY GUIDE, FOR SPACE	MX722LJ001
	EY7-0983-000	1	LED, GREEN	QLBLN342GN
	EY7-0984-000	4	KEY SWITCH, FOR CURSOR	SK0111X07A
	EY7-0985-000	1	KEY SWITCH, FOR SPACE	SK0111X09A
	EY7-0986-000	67	KEY SWITCH	SK0111X12A
	EY7-0987-000	1	KEY TOP ESC	VK122SH250
	EY7-0990-000	1	KEY TOP GRAPH	VK122SH253
	EY7-0991-000	1	KEY TOP SELECT	VK122SH254
	EY7-0992-000	1	KEY TOP 1	VK122SH268
	EY7-0993-000	1	KEY TOP 2	VK122SH269
	EY7-0994-000	1	KEY TOP 3	VK122SH270
	EY7-0995-000	1	KEY TOP 4	VK122SH271
	EY7-0996-000	1	KEY TOP 5	VK122SH272
	EY7-0997-000	1	KEY TOP 6	VK122SH273
	EY7-0998-000	1	KEY TOP 7	VK122SH274
	EY7-0999-000	1	KEY TOP 8	VK122SH275
	EY7-1000-000	1	KEY TOP 9	VK122SH276
	EY7-1001-000	1	KEY TOP 0	VK122SH277
	EY7-1002-000	1	KEY TOP ANGSTROM	VK122SH278
	EY7-1003-000	1	KEY TOP -	VK122SH279
	EY7-1004-000	1	KEY TOP >	VK122SH280
	EY7-1005-000	1	KEY TOP A	VK122SH281
	EY7-1006-000	1	KEY TOP Z	VK122SH282
	EY7-1007-000	1	KEY TOP E	VK122SH283

Key	Parts No.	Q'ty	Description	Remarks
	EY7-1008-000	1	KEY TOP R	VK122SH284
	EY7-1009-000	1	KEY TOP T	VK122SH285
	EY7-1010-000	1	KEY TOP Y	VK122SH286
	EY7-1011-000	1	KEY TOP U	VK122SH287
	EY7-1012-000	1	KEY TOP I	VK122SH288
	EY7-1013-000	1	KEY TOP O	VK122SH289
	EY7-1014-000	1	KEY TOP P	VK122SH290
	EY7-1015-000	1	KEY TOP ACCENT	VK122SH291
	EY7-1016-000	1	KEY TOP *	VK122SH292
	EY7-1017-000	1	KEY TOP Q	VK122SH293
	EY7-1018-000	1	KEY TOP S	VK122SH294
	EY7-1019-000	1	KEY TOP D	VK122SH295
	EY7-1020-000	1	KEY TOP F	VK122SH296
	EY7-1021-000	1	KEY TOP G	VK122SH297
	EY7-1022-000	1	KEY TOP H	VK122SH298
	EY7-1023-000	1	KEY TOP J	VK122SH299
	EY7-1024-000	1	KEY TOP K	VK122SH300
	EY7-1025-000	1	KEY TOP L	VK122SH301
	EY7-1026-000	1	KEY TOP M	VK122SH302
	EY7-1027-000	1	KEY TOP %	VK122SH303
	EY7-1028-000	1	KEY TOP #	VK122SH304
	EY7-1029-000	1	KEY TOP W	VK122SH305
	EY7-1030-000	1	KEY TOP X	VK122SH306
	EY7-1031-000	1	KEY TOP C	VK122SH307
	EY7-1032-000	1	KEY TOP V	VK122SH308
	EY7-1033-000	1	KEY TOP B	VK122SH309
	EY7-1034-000	1	KEY TOP N	VK122SH310
	EY7-1035-000	1	KEY TOP ,	VK122SH311
	EY7-1036-000	1	KEY TOP .	VK122SH312

Key	Parts No.	Q'ty	Description	Remarks
	EY7-1037-000	1	KEY TOP /	VK122SH313
	EY7-1038-000	1	KEY TOP +	VK122SH314
	EY7-1039-000	1	KEY TOP CAPS	VK122SH315
	EY7-1040-000	1	KEY TOP BS	VK122SH316
	EY7-1041-000	1	KEY TOP CODE	VK122SH317
	EY7-1062-000	3	KEY TOP INS, SUP, EFE	VK132SB009
	EY7-1064-000	1	KEY TOP TAB	VK132SH014
	EY7-1065-000	1	KEY TOP STOP	VK142SB004
	EY7-1066-000	1	KEY TOP CTRL	VK142SH006
	EY7-1069-000	1	KEY TOP RETURN	VK142SH009
	EY7-1070-000	2	KEY TOP CURSOR (LEFT, RIGHT)	VK143SH001
	EY7-1071-000	5	KEY TOP FUNCTION	VK152SB001
	EY7-1073-000	1	KEY TOP SHIFT (SMALL)	VK152SH003
	EY7-1074-000	1	KEY TOP SHIFT (LARGE)	VK162SH001
	EY7-1075-000	1	KEY TOP SPACE	VK172SH004
	EY7-1076-000	1	KEY TOP CURSOR (UP)	VK183SH001
	EY7-1077-000	1	KEY TOP CURSOR (DOWN)	VK183SH002
	EY7-1078-000	2	PLASTIC RIVET	VM163VB001
	EY7-1079-000	1	LED SHEET	VS115RB001
	EY7-1080-000	1	HOLDER PLATE, FOR FLAT CABLE	VS616VB002
	EY7-1081-000	1	CURSOR KEY FRAME	VS669SH001
	EY7-1082-000	2	KEY GUIDE HOLDER, FOR SPACE	VU111SB002
	EY7-1083-000	1	KEY GUIDE HOLDER, FOR SHIFT,CTRL	VU311SB001
	EY7-1084-000	8	KEY GUIDE HOLDER, FOR SHFT,RTN,FNCTN	VU411SB001
	EY7-1085-000	1	FLAT CABLE	WC17062AS1
	EY7-1086-000	1	JUNCTION JACK, FOR POWER LED	YJF02S044Z

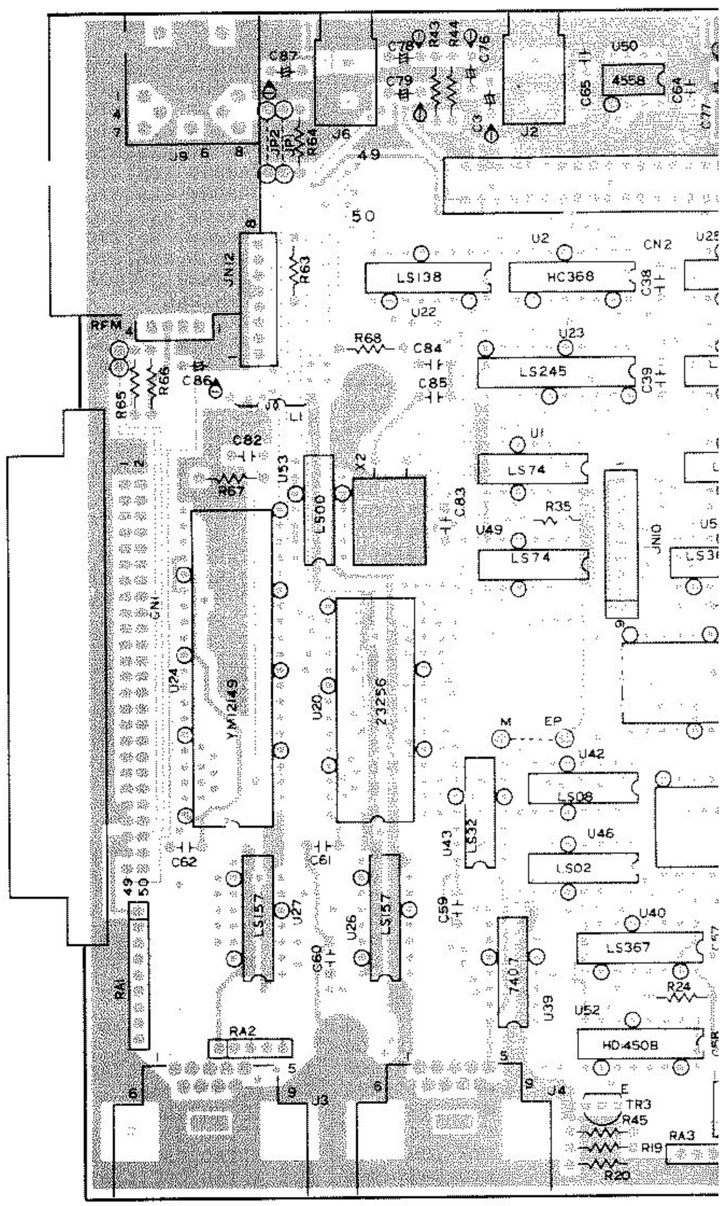
V-5. MAIN PCB PARTS

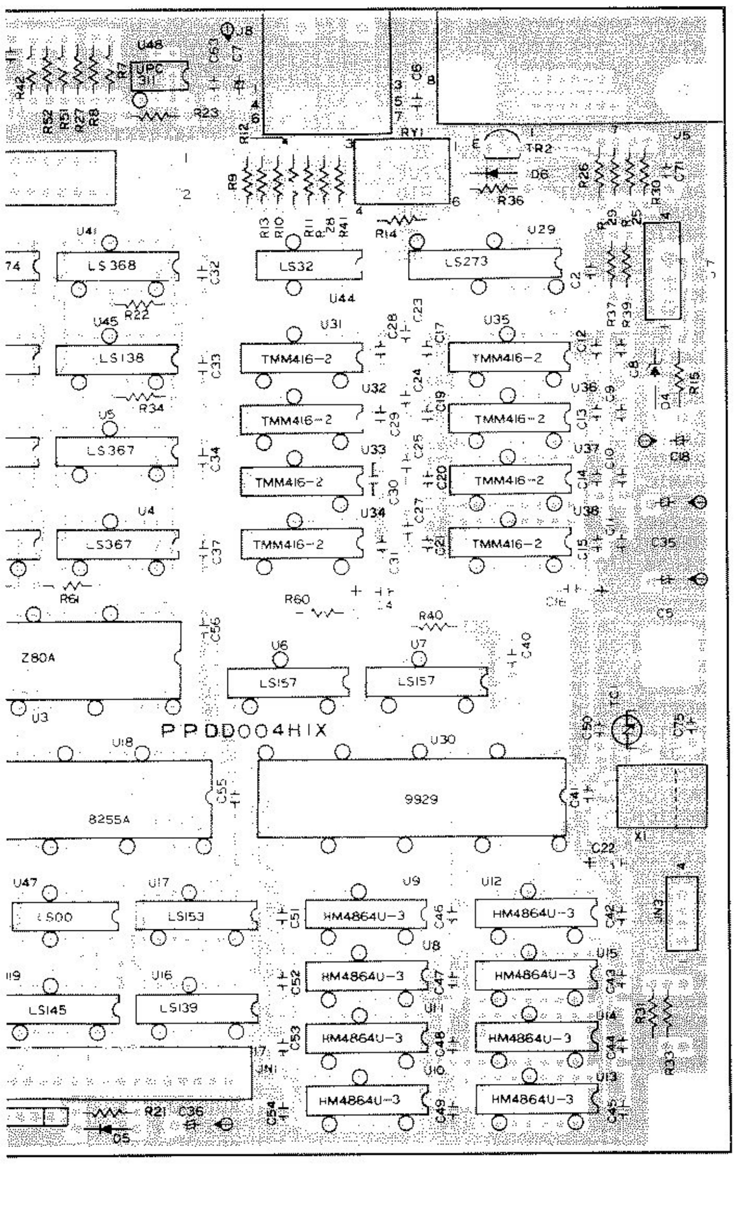
Key	Parts No.	Q'ty	Description	Remarks
	EY7-1104-000	2	SCREW M3X8 PAN HEAD, PLASTIC	BSPP3008NP
CN1	EY7-0922-000	1	JUNCTION JACK	YJF50S003Z
CN2	EY7-0923-000	1	JUNCTION JACK	YJF50S009Z
C2	VC4-3253-103	1	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C3	VC1-2161-106	1	ELECTRO. CAPACITOR 16V 10UF	CEVD100ALX
C4	EY7-0924-000	1	TANTALUM CAPACITOR 25V 4.7UF	CSVE4R7MLN
C5	VC1-2251-107	1	ELECTRO. CAPACITOR 25V 100UF	CEVE101ALX
C6	VC3-2501-223	1	MYLAR CAPACITOR 50V 0.022UF	CQMB223KTH
C7	VC1-2161-106	1	ELECTRO. CPACITOR 16V 10UF	CEVD100ALX
C8-11	VC4-3253-104	4	CERAMIC CAPACITOR 25V 0.1UF	CBF1E104ZT
C12-15	VC4-3253-103	4	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C16	EY7-0924-000	1	TANTALUM CAPACITOR 25V 4.7UF	CSVE4R7MLN
C17	VC4-3253-103	1	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C18	VC1-2161-106	1	ELECTRO CAPACITOR 16V 10UF	CEVD100ALX
C19-21	VC4-3253-103	3	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C22	EY7-0924-000	1	TANTALUM CAPACITOR 25V 4.7UF	CSVE4R7MLN
C23-25	VC4-3253-103	3	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C27	VC4-3253-103	1	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C28-31	VC4-3253-104	4	CERAMIC CAPACITOR 25V 0.1UF	CBF1E104ZT
C32-34	VC4-3253-103	3	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C35	VC1-1161-477	1	ELECTRO. CAPACITOR 16V 470UF	CEAD471ALX
C36	VC1-2161-226	1	ELECTRO. CAPACITOR 16V 22UF	CEVD220ALX
C37-40	VC4-3253-103	4	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C41-49	VC4-3253-104	9	CERAMIC CAPACITOR 25V 0.1UF	CBF1E104ZT
C50	VC4-2502-330	1	CERAMIC CAPACITOR 50V 33PF	CCGB330K0T
C51-54	VC4-3253-103	4	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C55/56	VC4-3253-104	2	CERAMIC CAPACITOR 25V 0.1UF	CBF1E104ZT
C57-61	VC4-3253-103	5	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C62	VC4-3253-104	1	CERAMIC CAPACITOR 25V 0.1UF	CBF1E104ZT
C63-65	VC4-3253-103	3	CERAMIC CAPACITOR 25V 0.01UF	CBF1E103KT
C71	VC3-2501-223	1	MYLAR CAPACITOR 50V 0.022UF	CQMB223KTH
C75	VC4-2502-120	1	CERAMIC CAPACITOR 50V 12PF	CCGB120K0T
C76-79	VC1-2161-106	4	ELECTRO. CAPACITOR 16V 10UF	CEVD100ALX
C80	VC3-2501-152	1	MYLAR CAPACITOR 50V 1500PF	CQMB152KTH
C81	VC3-2501-102	1	MYLAR CAPACITOR 50V 1000PF	CQMB102KTH
C82/83	VC4-2502-330	2	CERAMIC CAPACITOR 50V 33PF	CCGB330K0T
C84/85	VC4-3503-221	2	CERAMIC CAPACITOR 50V 220PF	CCGB221K0T
C86	VC1-2161-336	1	ELECTRO. CAPACITOR 16V 33UF.....[UK]	CEVD330ALX
C87	VC1-2161-107	1	ELECTRO. CAPACITOR 10V 100UF.....[UK]	CEVD101ALX
D4	EY7-0925-000	1	ZENER DIODE 05Z4.7 OR 05Z5.1 X,Y	QDZ05ZXXXT
D5/D6	X65-5435-000	2	SILICON DIODE 1S2076	QDSS2076#B
JN1	EY7-0927-000	1	JUNCTION JACK	YJF17S010Z
JN3	EY7-0928-000	1	JUNCTION JACK	YJF04S043Z
JN10	EY7-1099-000	1	JUNCTION JACK.....[UK]	YJF09S107Z
JN11	EY7-1098-000	1	JUNCTION JACK.....[FRENCH]	YJF08S108Z
JN12	EY7-1098-000	1	JUNCTION JACK.....[FRENCH]	YJF08S108Z
J2	EY7-0929-000	1	PIN JACK (2 PIN)	YJP02S017Z
J3/4	EY7-0930-000	2	JUNCTION JACK	YJF09S106Z
J5	EY7-0931-000	1	JUNCTION JACK	YJF14S034Z
J6	EY7-0929-000	1	PIN JACK (2 PIN).....[UK]	YJP02S017Z
J7	EY7-0932-000	1	JUNCTION JACK	YJF04S038Z
J8	EY7-0933-000	1	JUNCTION JACK	YJF08S033Z
J9	EY7-1097-000	1	JUNCTION JACK .....[FRENCH]	YJD08S010Z
L1	EY7-1094-000	1	RF COIL.....[UK]	LF220KE07Y
RA1	EY7-0934-000	1	RESISTOR ARRAY 1/8W 10KX8	RAB103K08N
RA2	EY7-0935-000	1	RESISTOR ARRAY 1/8W 10KX4	RAB103K04N
RA3	EY7-0934-000	1	RESISTOR ARRAY 1/8W 10KX8	RAB103K08N
RFM	EY7-0970-000	1	RF MODULATOR.....[UK]	ZUU0000004
RY1	EY7-0936-000	1	RELAY	ZRA265102Z
R7	VR1-1143-102	1	CARBON RESISTOR 1/4W 1K	RD25PJ102X
R8	VR1-1143-224	1	CARBON RESISTOR 1/4W 220K	RD25PJ224X
R9	VR1-1143-472	1	CARBON RESISTOR 1/4W 4.7K	RD25PJ472X
R10/11	VR1-1143-103	2	CARBON RESISTOR 1/4W 10K	RD25PJ103X
R12	VR1-1143-474	1	CARBON RESISTOR 1/4W 470K	RD25PJ474X
R13/14	VR1-1143-272	2	CARBON RESISTOR 1/4W 2.7K	RD25PJ272X
R15	VR1-1123-471	1	CARBON RESISTOR 1/2W 470 OHM	RD50TJ471X
R19	VR1-1143-102	1	CARBON RESISTOR 1/4W 1K	RD25PJ102X
R20	VR1-1143-473	1	CARBON RESISTOR 1/4W 47K	RD25PJ473X
R21	VR1-1143-103	1	CARBON RESISTOR 1/4W 10K	RD25PJ103X
R22,23	VR1-1143-472	2	CARBON RESISTOR 1/4W 4.7K	RD25PJ472X

V-4. MAIN PCB ASSEMBLY DIAGRAM

* This diagram shows the view seen from the top surfasce.

** RFM is not mounted in French version.




U48
UPC 311
R23
J8
RY1
TR2
D6
R36
J5
U41
LS368
U44
LS32
R14
U29
LS273
R22
U45
LS138
U31
TMM416-2
U35
TMM416-2
R34
U32
TMM416-2
U36
TMM416-2
U5
LS367
U33
TMM416-2
U37
TMM416-2
U4
LS367
U34
TMM416-2
U38
TMM416-2
C35
R61
R60
R40
C5
Z80A
U6
LS157
U7
LS157
U3
PPDD004H1X
U18
8255A
U30
9929
X1
U47
LS00
U17
LS153
U9
HM4864U-3
U12
HM4864U-3
JN3
U8
HM4864U-3
U15
HM4864U-3
U16
LS145
LS139
U11
HM4864U-3
U14
HM4864U-3
JN1
U10
HM4864U-3
U13
HM4864U-3
R21
C36
D5

Key	Parts No.	Q'ty	Description	Remarks
R24	VR1-1143-103	1	CARBON RESISTOR 1/4W 10K	RD25PJ103X
R25	VR1-1143-472	1	CARBON RESISTOR 1/4W 4.7K	RD25PJ472X
R26	VR1-1143-101	1	CARBON RESISTOR 1/4W 100 OHM	RD25PJ101X
R27	VR1-1143-471	1	CARBON RESISTOR 1/4W 470 OHM	RD25PJ471X
R28	VR1-1143-472	1	CARBON RESISTOR 1/4W 4.7K	RD25PJ472X
R29	VR1-1143-102	1	CARBON RESISTOR 1/4W 1K	RD25PJ102X
R30	VR1-1143-472	1	CARBON RESISTOR 1/4W 4.7K	RD25PJ472X
R31/33	VR1-1143-221	2	CARBON RESISTOR 1/4W 220 OHM	RD25PJ221X
R34	VR1-1143-103	1	CARBON RESISTOR 1/4W 10K	RD25PJ103X
R35	VR1-1143-821	1	CARBON RESISTOR 1/4W 820 OHM	RD25PJ821X
R36	VR1-1143-103	1	CARBON RESISTOR 1/4W 10K	RD25PJ103X
R37/39	VR1-1143-102	2	CARBON RESISTOR 1/4W 1K	RD25PJ102X
R40/41	VR1-1143-102	2	CARBON RESISTOR 1/4W 1K	RD25PJ102X
R42	VR1-1143-272	1	CARBON RESISTOR 1/4W 2.7K	RD25PJ272X
R43	VR1-1143-472	1	CARBON RESISTOR 1/4W 4.7K	RD25PJ472X
R44	VR1-1143-203	1	CARBON RESISTOR 1/4W 20K	RD25PJ203X
R45	VR1-1143-104	1	CARBON RESISTOR 1/4W 100K	RD25PJ104X
R51	VR1-1143-101	1	CARBON RESISTOR 1/4W 100 OHM	RD25PJ101X
R52	VR1-1143-562	1	CARBON RESISTOR 1/4W 5.6K	RD25PJ562X
R60/61	VR1-1143-332	1	CARBON RESISTOR 1/4W 3.3K	RD25PJ332X
R62	VR1-1143-182	1	CARBON RESISTOR 1/4W 1.8K	RD25PJ182X
R63	VR1-1143-102	1	CARBON RESISTOR 1/4W 1K.....[FRENCH]	RD25PJ102X
R64	VR1-1143-680	1	CARBON RESISTOR 1/4W 68 OHM.....[UK]	RD25PJ680X
R65/66	VR1-1143-182	2	CARBON RESISTOR 1/4W 1.8K.....[UK]	RD25PJ182X
R67/68	VR1-1143-102	2	CARBON RESISTOR 1/4W 1K	RD25PJ102X
R71	VR1-1143-102	1	CARBON RESISTOR 1/4W 1K	RD25PJ102X
TC1	EY7-0938-000	1	TRIMMER CAPACITOR	CTZ5250H01
TP	EY7-0926-000	1	TERMINAL	YZC1150001
TR2	EY7-0939-000	1	TRANSISTOR 2SA720 R-RANK	QTA0720XDN
TR3	EY7-0940-000	1	TRANSISTOR 2SC2603 NO-RANK	QTC2603XUE
U1	WA3-0137-000	1	IC SN74LS74AN	QQT07474AU
U2	EY7-0941-000	1	IC MN74HC368	QQ074368AN
U3	EY7-0944-000	1	IC UPD780-1	QQN00780AA
U4/5	WA3-0198-000	2	IC SN74LS367AN	QQT74367AU
U6/7	X65-7468-000	2	IC SN74LS157N	QQT74157AU
U8-15	WA3-0698-000	8	IC HM4864U-3	QQN04864CB
U16	WA3-0200-000	1	IC SN74LS139N	QQT74139BU
U17	WA3-0283-000	1	IC SN74LS153N	QQT74153DU
U18	WA3-0944-000	1	IC UPD8255A-5	QQNO8255BA
U19	WA3-0141-000	1	IC SN74LS145N	QQT74145CU
U20	EY7-0942-000	1	IC HN613256PM87.....[FRENCH]	QQ061325XB
	EY7-1095-000	1	IC HN613256PM67.....[UK]	QQ061325WB
U21	WA3-0137-000	1	IC SN74LS74AN	QQT07474AU
U22	WA3-0110-000	1	IC SN74LS138N	QQT74138AU
U23	WA3-0361-000	1	IC SN74LS245N	QQT74245AU
U24	EY7-0943-000	1	IC YM-2149	QQN02149AZ
U25	WA3-0137-000	1	IC SN74LS74AN	QQT07474AU
U26/27	X65-7468-000	2	IC SN74LS157N	QQT74157AU
U28	WA3-0135-000	1	IC SN74LS32N	QQT07432BU
U29	WA3-0279-000	1	IC SN74LS273N	QQT74273AU
U30	EY7-0945-000	1	IC TMS-9929A	QQM09929AU
U31-38	EY7-0946-000	8	IC TMM-416-2	QQN00416AT
U39	X65-7336-000	1	IC SN7407N	QQT07407BU
U40	WA3-0198-000	1	IC SN74LS367AN	QQT74367AU
U41	WA3-0145-000	1	IC HD74LS368AP	QQT74368AB
U42	WA3-0134-000	1	IC SN74LS08N	QQT07408BU
U43/44	WA3-0135-000	2	IC SN74LS32N	QQT07432BU
U45	WA3-0110-000	1	IC SN74LS138N	QQT74138AU
U46	WA3-0148-000	1	IC SN74LS02N	QQT07402BU
U47	WA3-0132-000	1	IC SN74LS00N	QQT07400BU
U48	EY7-0947-000	1	IC UPC311	QQM00311AA
U49	WA3-0137-000	1	IC SN74LS74AN	QQT07474AU
U50	EY7-0948-000	1	IC NJM4558D	QQM04558AJ
U51	WA3-0198-000	1	IC SN74LS367AN	QQT74367AU
U52	WA3-0911-000	1	IC TC4050BP	QQ004050CT
U53	WA3-0132-000	1	IC SN74LS00N	QQT07400BU
X1	EY7-0949-000	1	X'TAL OSCILLATOR.....[FRENCH]	XAZ1C5001X
X1	EY7-1096-000	1	X'TAL OSCILLATOR.....[UK]	XAZ3A3001X
X2	EY7-0937-000	1	X'TAL OSCILLATOR	XBR1A1007X
	EY7-1100-000	1	RGB ENCODER PCB.....[FRENCH]	ZUW0000002
	EY7-1101-000	1	PAL ENCIDER PCB.....[UK]	ZUW0000003

V-6. MAIN PCB ASSEMBLY DIAGRAM

This diagram shows the view seen from the top surface.

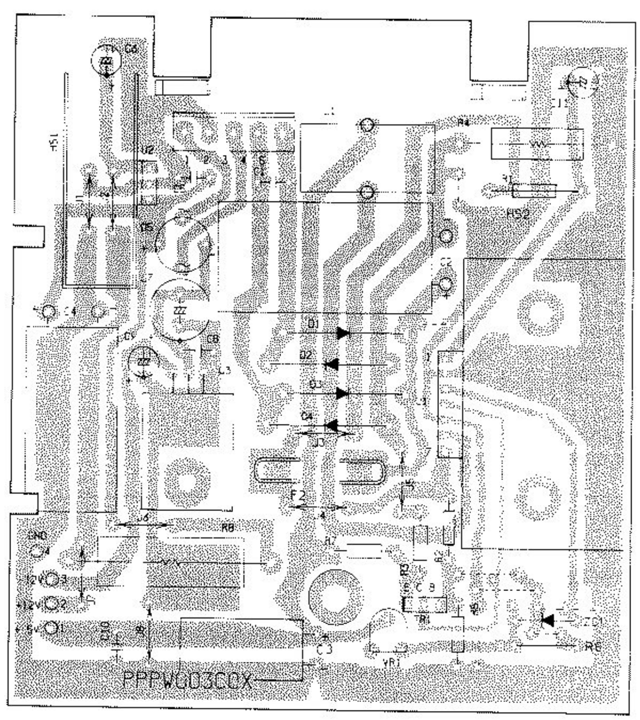


Fig. V-3

V-7. POWER PCB PARTS

Key	Parts No.	Q'ty	Description	Remarks
	EY7-0952-000	1	CONNECTOR CORD ASSY	ACCNP09GEA
	XB7-2200-307	3	NUT, M3	BNHCL30NSZ
	XB6-6300-805	1	SCREW, M3X8 CEMS	BSPC3008NZ
	XB6-6301-205	2	SCREW, M3X12 CEMS	BSPC3012NZ
	EY7-1105-000	1	SCREW, M3X8 TAPPING	BTPW3008AZ
	EY7-0953-000	2	FUSE HOLDER	YHF0P0001Z
CN1	EY7-0954-000	1	JUNCTION JACK	YJF05S017Z
C1	EY7-0956-000	1	CERAMIC CAPACITOR 50V 0.1UF	CBF1H104ZT
C2	VC1-1251-478	1	ELECTRO. CAPACITOR 25V 4700UF	CEAE472UMN
C3	VC1-1161-108	1	ELECTRO. CAPACITOR 16V 1000UF	CEAD102UMN
C4	VC1-1251-338	1	ELECTRO. CAPACITOR 25V 3300UF	CEAE332UMN
C5	EY7-0969-000	1	MYLAR CAPACITOR 50V 0.01UF	CQMB103KTH
C6	VC1-2501-105	1	ELECTRO. CAPACITOR 50V 1UF	CEVG010ALX
C7	VC1-1351-227	1	ELECTOR. CAPACITOR 35V 220UF	CEAF221UMN
C8	EY7-0969-000	1	MYLAR CAPACITOR 50V 0.01UF	CQMB103KTH
C9	VC1-2501-105	1	ELECTRO. CAPACITOR 50V 1UF	CEVG010ALX
C10	EY7-0956-000	1	CERAMIC CAPACITOR 50V 0.1UF	CBF1H104ZT
C11	VC1-2501-106	1	ELECTRO. CAPACITOR 50V 10UF	CEVG100ALX
D1-4	EY7-0957-000	4	DIODE S2V-10	QDS2V10XXK
D5	EY7-0958-000	1	DIODE 1B4B1-D	QDS1B4B1XT
F2	EY7-0959-000	1	FUSE 2.5A	ZFBP25204K
L1	EY7-0960-000	1	TROIDAL COIL	LWS151301T
R1	VR1-1123-472	1	CARBON RESISTOR 1/2W 4.7K	RD50TJ472X
R2	VR1-1143-105	1	CARBON RESISTOR 1/4W 1M	RD25PJ105X
R3	VR1-1143-101	1	CARBON RESISTOR 1/4W 100 OHM	RD25PJ101X
R4	EY7-0961-000	1	CEMENT RESISTOR 2W 0.22 OHM	RF02SKR22B
R5	VR1-1143-123	1	CARBON RESISTOR 1/4W 12K	RD25PJ123X
R6	VR1-1143-471	1	CARBON RESISTOR 1/4W 470 OHM	RD25PJ471X
R7	VR1-1143-152	1	CARBON RESISTOR 1/4W 1.5K	RD25PJ152X
R8	EY7-0962-000	1	CEMENT RESISTOR 3W 56 OHM	RF03SK560B
TR1	EY7-0963-000	1	TRANSISTOR 2SC2603 NO-RANK	QTC2603XHE
U1	EY7-0964-000	1	IC STK770	QQHSK770AC
U2	EY7-0965-000	1	IC AN7812	QQM07812AN
U3	EY7-0966-000	1	IC NJM7912A	QQM07912BJ
VR1	EY7-0967-000	1	VR 500 OHM B-CURVE	RPSNB50105
ZD1	EY7-0968-000	1	ZENER DIODE 4.9-5.3V	QDZHZ2CLXB

VI-2. POWER SUPPLY SECTION CIRCUIT DIAGRAM

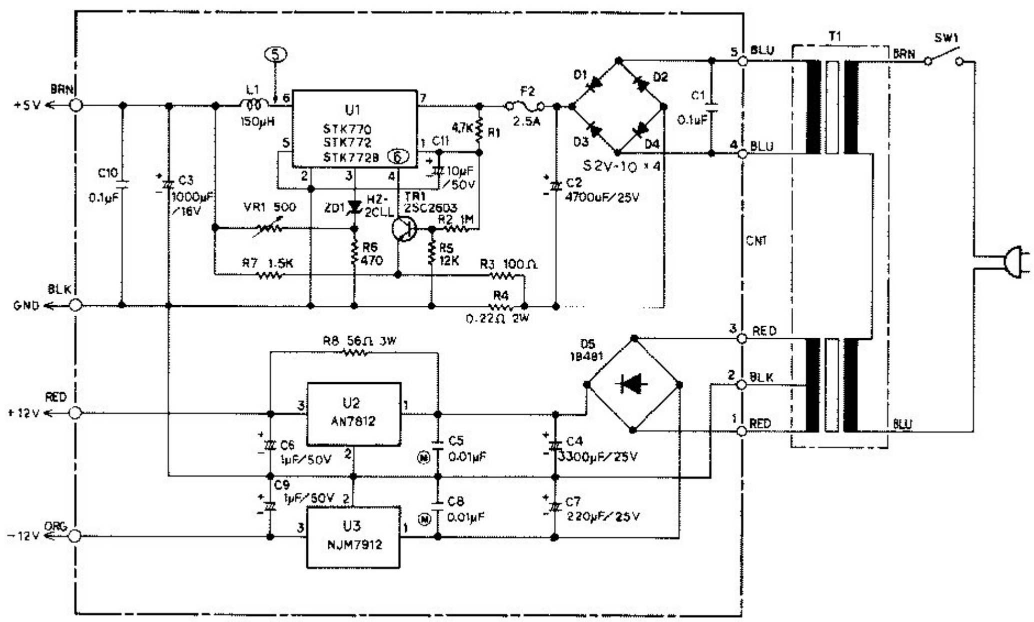


Fig. VI-2

Notes:

Circuits and parts may be changed without prior notice due to improvements.

Capacitors

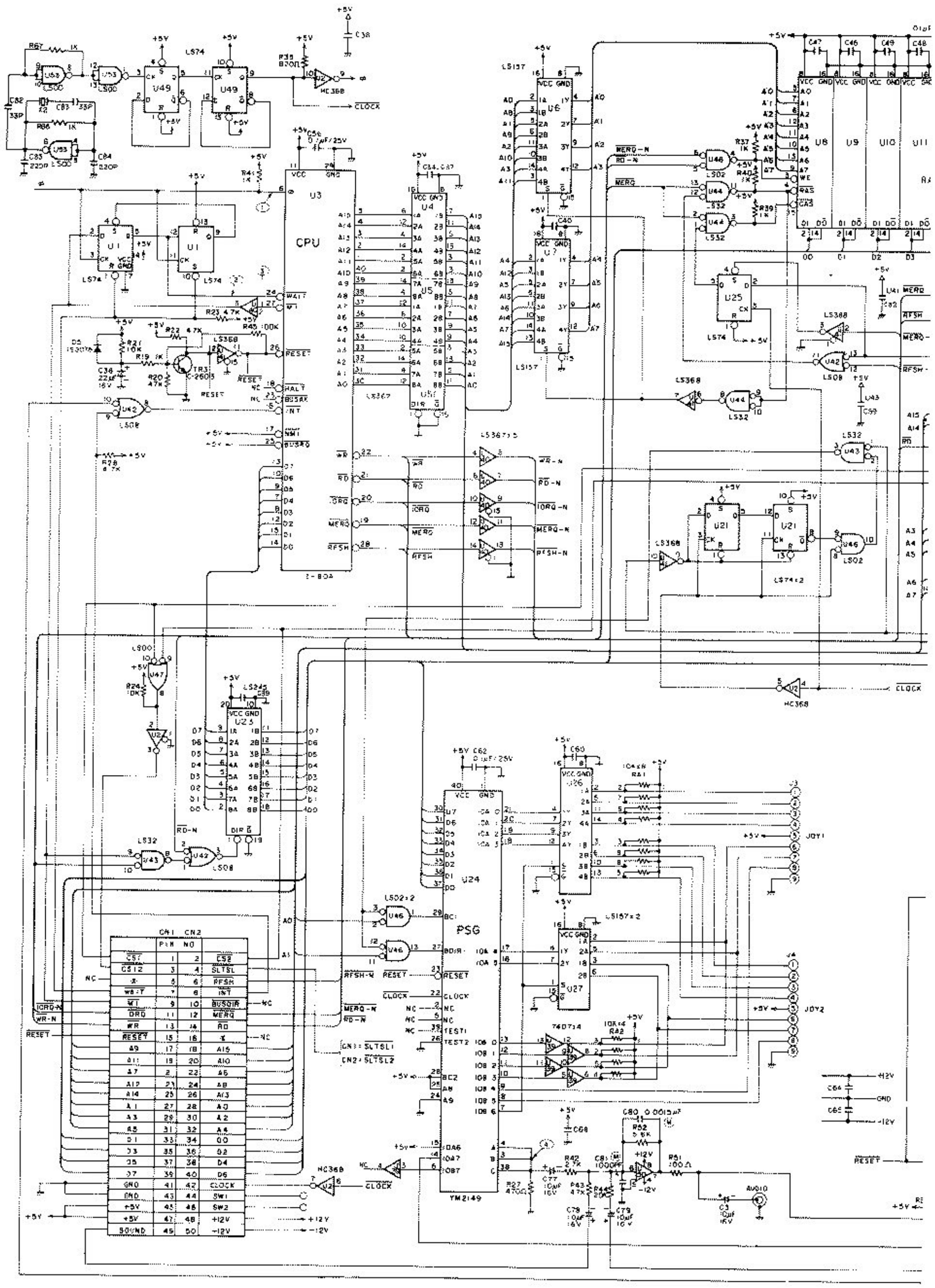
(1) All capacitors without polarity markings are ceramic capacitors unless otherwise indicated.
(2) All capacitors without constant markings are 0.01 μF/25 V ceramic capacitors.
(3) (M) indicates Mylar capacitors.
(4) Electrolytic capacitors marked (T) are tantalum capacitors.

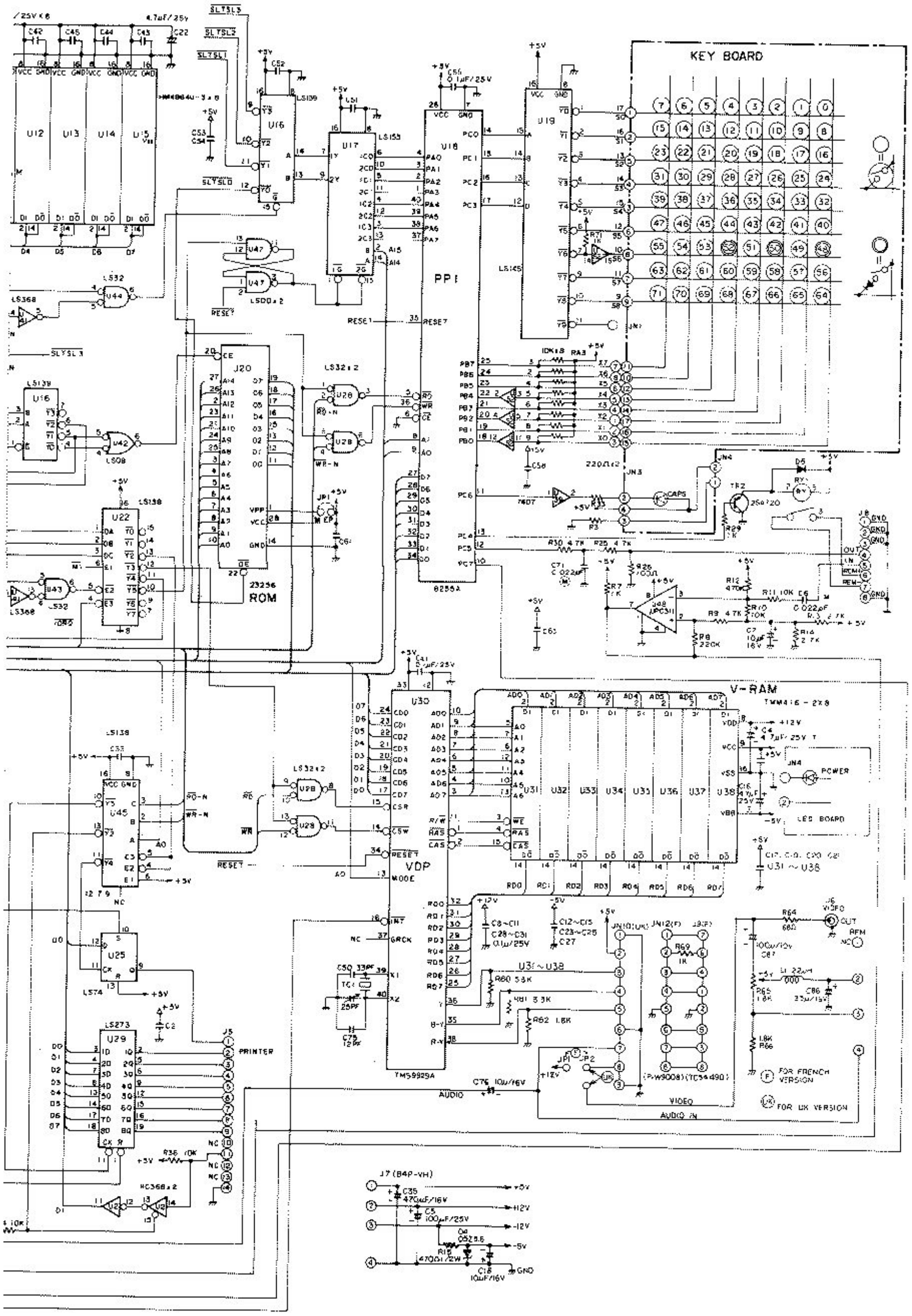
Resistors

(1) All resistors are 1/4 W, ±5% carbon resistors unless otherwise indicated.

VI. CIRCUIT DIAGRAM

VI-1. MAIN PCB CIRCUIT DIAGRAM




KEY BOARD
PPI
8255A
ROM
23256
V-RAM
TMM416 - 2X8
VDP
TMS9929A
PRINTER
POWER
LED BOARD
VIDEO
AUDIO
AUDIO IN
FOR FRENCH VERSION
FOR UK VERSION
J7 (B4P-VH)

VI-3. WAVEFORMS

* Given below are photos of waveforms taken at prominent locations in the circuitry. The actual measurement point is indicated by the number enclosed in the oval on the circuit diagrams.

(1) Pin 6 of CPU (ϕ)
2 V/div. 0.1 μsec/div.

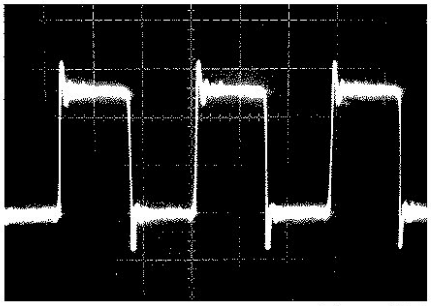


Photo VI-1

(2) Pin 24 of CPU ($\overline{\text{WAIT}}$)
2 V/div. 1 μsec/div.

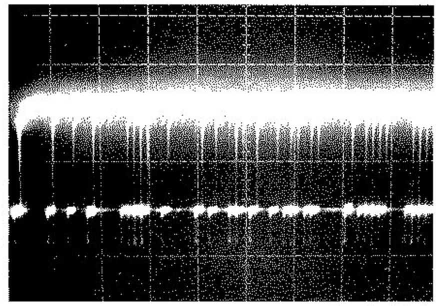


Photo VI-2

(3) Pin 27 of CPU ($\overline{\text{M1}}$)
1 V/div. 1 μsec/div.

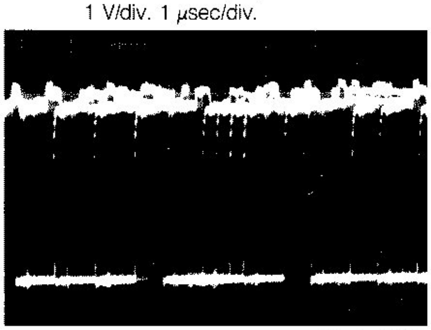


Photo VI-3

(4) Pin 3 of PSG (Refer to note below)
500 mV/div. 2 μsec/div.

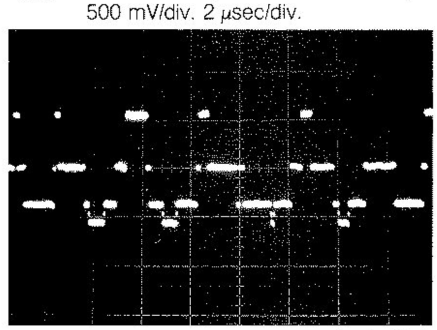


Photo VI-4

(5) Pin 6 of U1 (Power PCB)
5 V/div. 10 μsec/div.

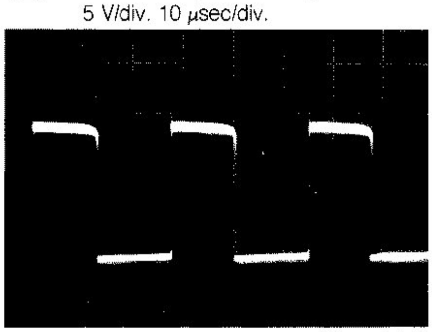


Photo VI-5

(6) Pin 4 of U1 (Power PCB)
5 V/div. 10 μsec/div.

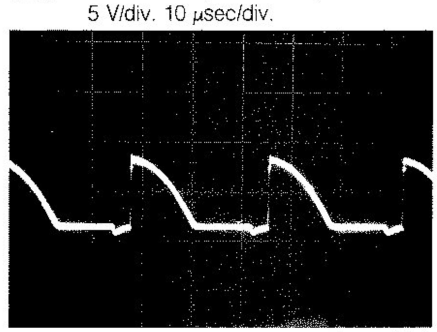


Photo VI-6

Note:
Waveform when 3-tone cord is output with following program.
10 PLAY "V15T100L104C", "V15T100L104E", "V15T100L104G"
20 GOTO 10

VII. KEYBOARD

VII-1. KEYBOARD MATRIX

UK version

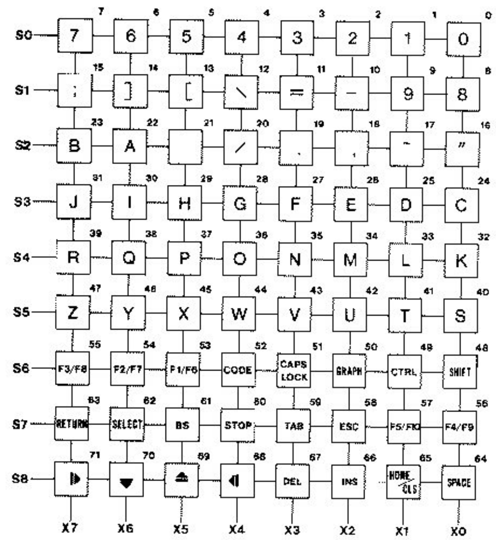


Fig. VII-1

French version

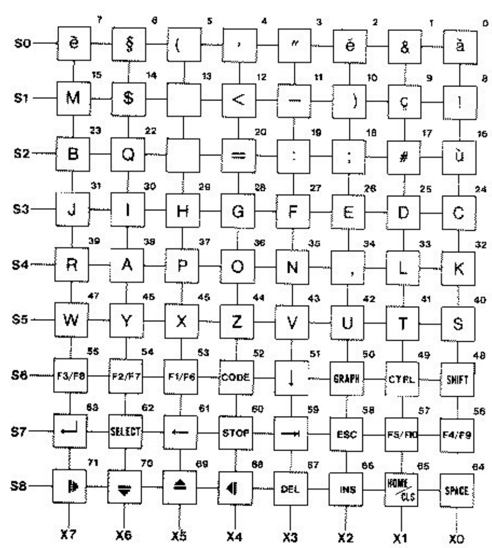


Fig. VII-2

VII-2. KEY INPUT MODES

* When no special key is used.

UK version

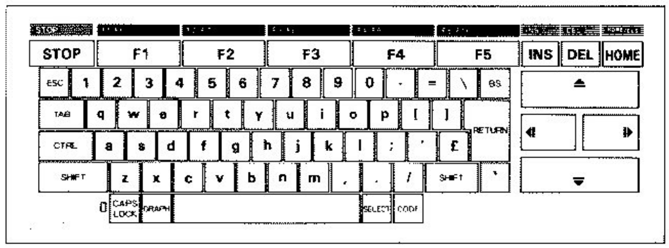


Fig. VII-3

French version

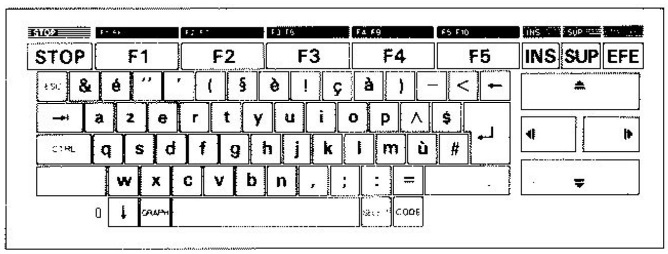


Fig. VII-4

* With the SHIFT Key is pressed.

UK version

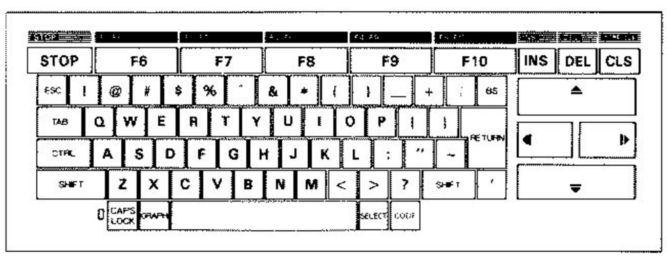


Fig. VII-5

French version

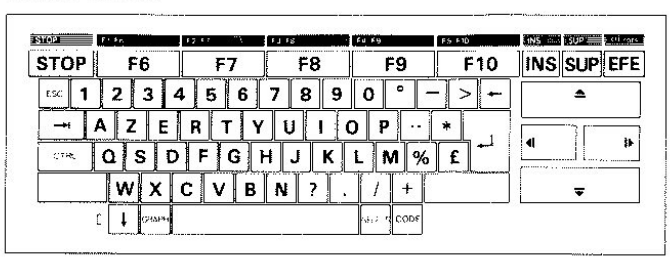


Fig. VII-6

* When the CODE key is pressed.

UK version

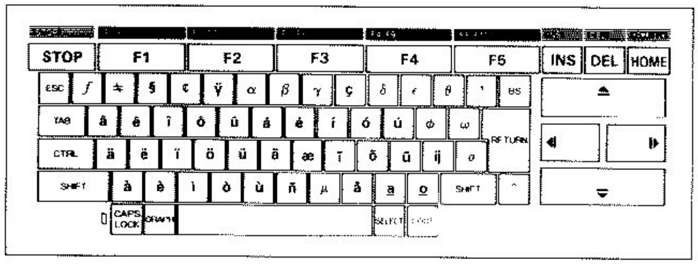


Fig. VII-7

French version

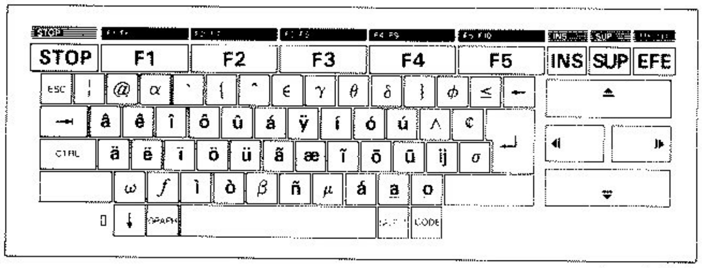


Fig. VII-8

* When the CODE and SHIFT keys are pressed.

UK version

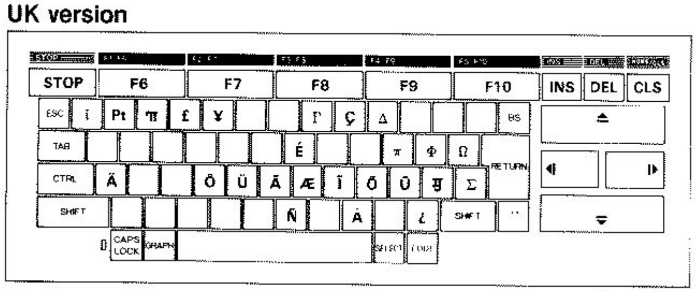


Fig. VII-9

French version

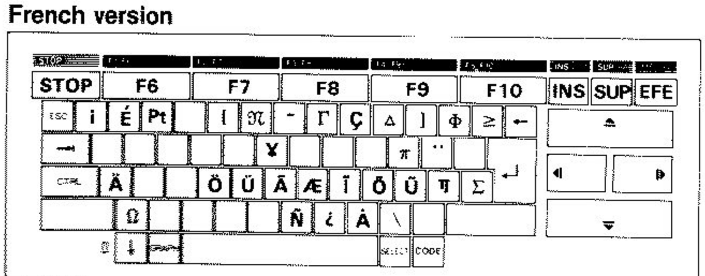


Fig. VII-10

* When the GRAPH key is pressed.

UK version

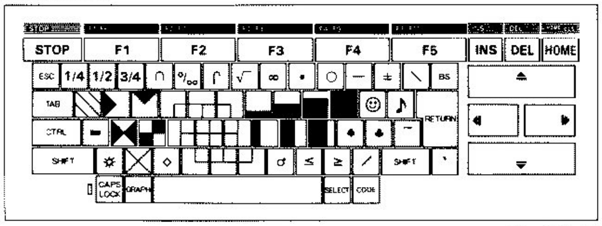


Fig. VII-11

French version

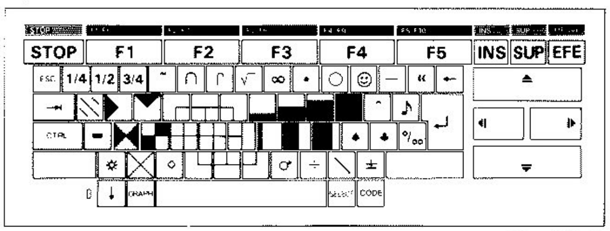


Fig. VII-12

* When the GRAPH and SHIFT keys are pressed.

UK version

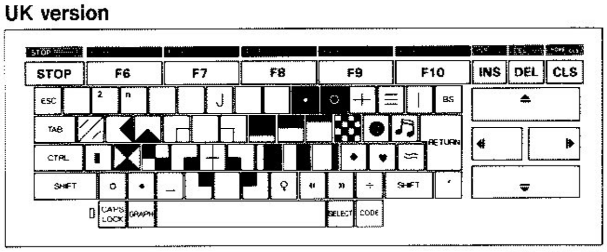


Fig. VII-13

French version

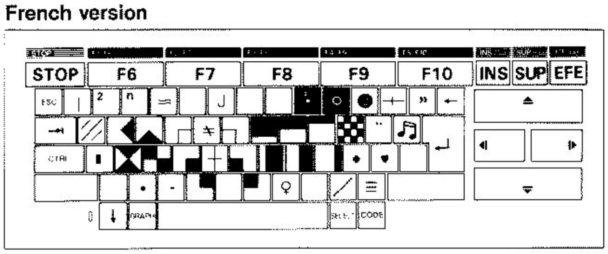


Fig. VII-14

VIII. APPENDIX

VIII-1. PAL ENCODER CIRCUIT DIAGRAM (UK version)

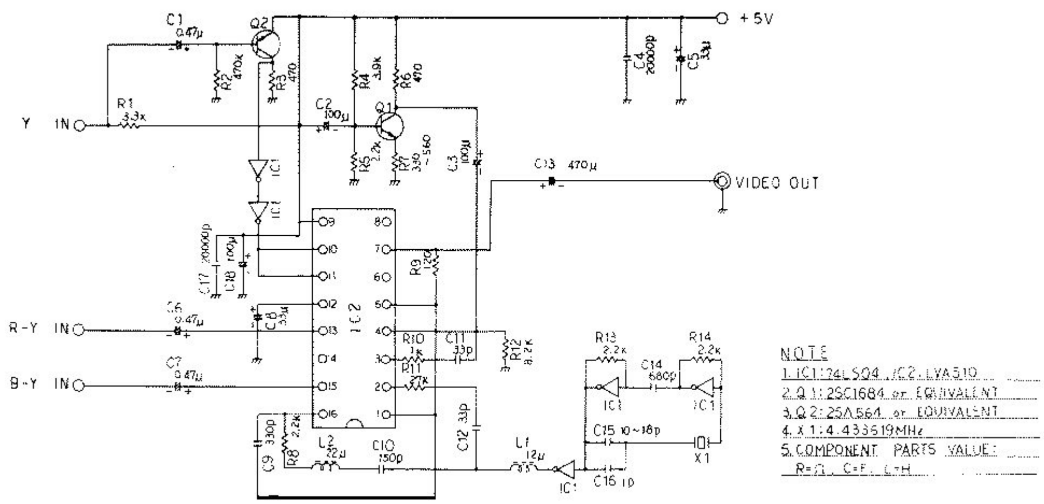


Fig. VIII-1

VIII-2. RGB ENCODER CIRCUIT DIAGRAM (French version)

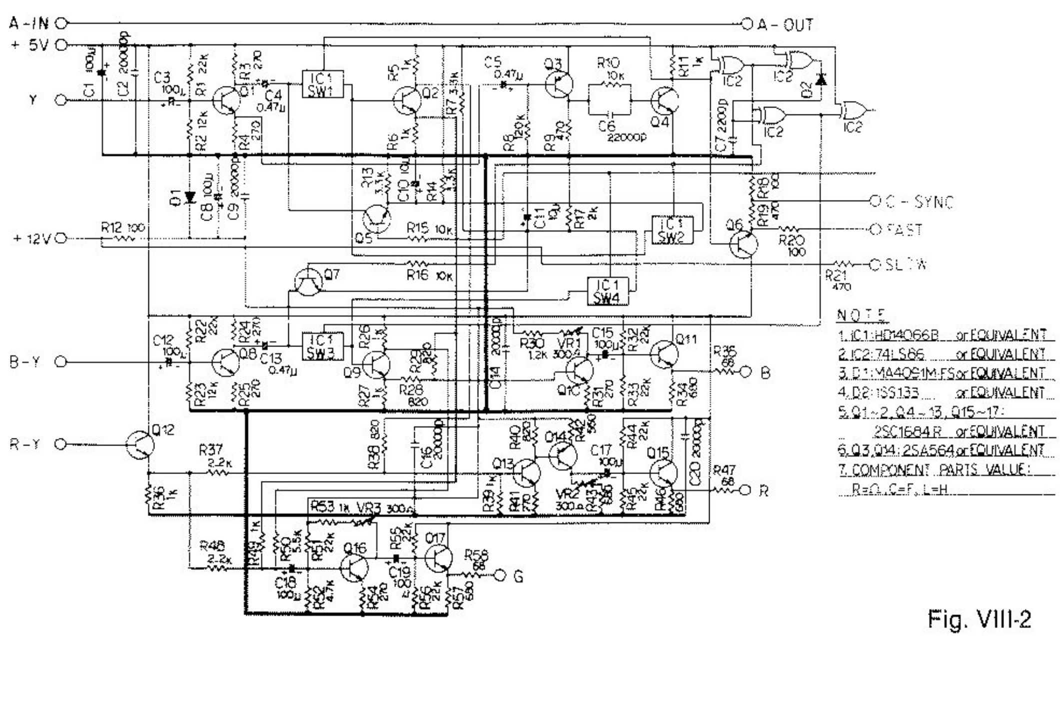


Fig. VIII-2

VIII-3. PAL ENCODER ASSEMBLY DIAGRAM (UK version)

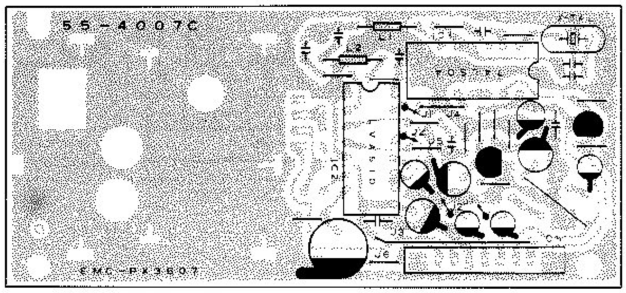


Fig. VIII-3

VIII-4. RGB ENCODER ASSEMBLY DIAGRAM (French version)

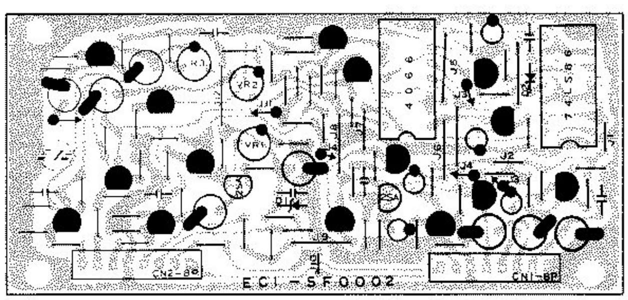


Fig. VIII-4